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P833

CASSETTE CONTROL UNIT

(FIRST DRAFT).

PRELIMINARY INFORMATION.

SECTION III

P833 CASSETTE TAPE CONTROL UNIT

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SECTION III

P833 CASSETTE TAPE CONTROL UNIT

3.1. INTRODUCTION

The P833 Cassette Tape Control Unit provides a control interface between a P855/60/50 central processor and up to four Philips Professional Cassette Drives. The control unit can be connected to the central processor via the standard I/O bus for operation on the Programmed Channel (with or without interrupt) or on the Multiplex Channel. A block diagram of a typical cassette tape subsystem is shown in Figure 3.1.

3.2. DEVICE. The device handled by the P833 control unit is the Philips Professional Cassette Drive type ELA K7 which uses Philips type Professional Cassettes. Table 3.1 gives brief device specifications. Additional device information is given in the manufacturer's manual.

3.3. PHYSICAL. The cassette control unit consists of three printed circuit cards mounted together with the power supply modules and the I/O Extender card in a standard 5-card rack. A detailed physical description, including all interconnections, is given later in this section (see paragraph 3.65).

3.4 REFERENCE INFORMATION. General information about the P855/60/50 input/output facilities is given in Section I of this manual.

This control unit description is based on the following documents:

Boolean Book	059 CADOLI 14473.58 , rum 3437 , date 730130 12NC: 5111 991 03872
Cablage Specification	12NC : 5111 199 83831 date 721012 mod. A1600
Definition des Liasons	12NC : 5111 199 83931 , date 720914.

Table 3.1 Device Specifications

Characteristic	Description
Head type	Single track, read-after-write (one head with two gaps).
Recording technique	Character serial, bit serial, phase encoded.
Recording density	800 bpi. → bits
Tape speed	19cm/s ($7\frac{1}{2}$ ips).
Data transfer rate	750 characters/second.
Start time/distance	40 msec / 7 mm (0.28 in).
Stop time/distance	20 msec / 2 mm (0.08 in).
Max. rewind time	45 seconds.
Cassette type	Twin hub coplanar, metal frame work.
Tape type/size	Magnetic tape, 86 m (282 ft) long.
Tape data capacity	2.8 million bits on each track.
Number of tracks	One ~~for~~ at each cassette side.
Tape side identifiers	Asymmetrically positioned cutout in rear edge of cassette frame.
Tape markers	Two ~~strong~~ holes for BOT/EOT detection by optical means. (approx. 10 cm from bot/eot) 45 cm from — leader
File protect	Two replaceable write enable plugs in cut-outs at rear edge of cassette frame..

3.5. ORGANIZATION. Information on tape is arranged in bit-serial, character-serial format. The characters are of 8 bits and are organized into blocks consisting of a Preamble character, up to 256 data characters and a Postamble character. Figure 3.2 illustrates the track layout.

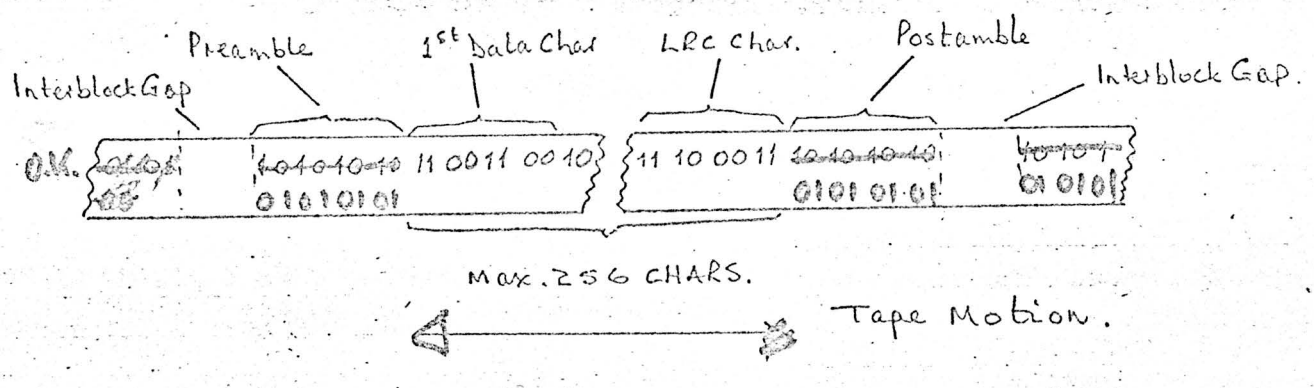


Figure 3.2. Data Organization

3.6. Preamble/Postamble Characters. The Preamble and Postamble characters have the same bit pattern $(01010101)_2$ and are the first and last characters, respectively, of a block. They are hardware generated within the control unit and are not normally sent to the central processor during read operations. The Postamble character can be transferred if the programmed block length is greater than the physical length of the record.

3.7 LRC Character. The cassette subsystem uses a Longitudinal Redundancy Check (LRC) character to detect data errors when reading and writing. The LRC character is software generated and must be programmed as the last data character of a block; it immediately precedes the Postamble character. During read and read-after-write operations the serial data read from tape is hardware checked by the control unit and if the final data character does not correspond to the LRC character a data fault indication occurs.

3.8. FUNCTIONAL DESCRIPTION

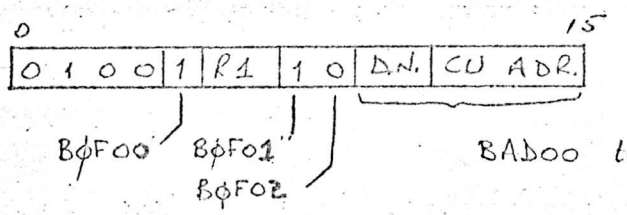
The following description refers to drawings and timing diagrams included with the general text and to the logic diagrams at the end of the section. A block diagram of the control unit is given at the end of this part (Figure 3.13). Basic I/O bus information and information common to the P855/60 range of high speed control units is included in Section I of this manual.

3.9. ADDRESSING. The CU address and device number are specified on the BAD00/ to BAD05/ lines which are activated whenever a command is received by the CU. BAD00/ and BAD01/ specify the device number and are set into the BAD flip-flops at the start of every command. BAD02/ to BAD05/ contain the CU address and must be decoded by the CU. They are compared with the hard-wired CU address preset at system installation time by means of four jumpers on circuit card B (see paragraph 3.68). A correct CU address code on the BAD lines, along with the Device Address Validation (DAV/) signal which is activated during every command period, generates the Addressed Recognised (ARE/) signal to the CPU.

3.10. I/O COMMANDS. The CU recognises and responds to the six types of P855/60 I/O commands described in the following paragraphs. These commands are transferred to the control unit on the BOF00/ to BOF02/ lines and are always accompanied by the address information (see paragraph 3.9.). The TST, SST and CIO commands are transferred from the CPU on the Programmed Channel. The INR and OTR commands may be transferred on the Programmed Channel or on the Multiplex Channel.

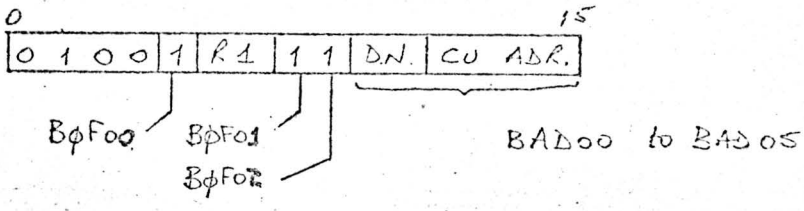
3.11. Command Accept. When an I/Ø command is received, the BØF lines are decoded if the address is correct (Figure 3.26, AREA/ low). The corresponding output from COMMAND produces the Command Accept (ACC/) signal which is returned to the CPU.

3.12. TEST STATUS (TST).



Test Status (TST). This command is used by the CPU to test the status of the CU before beginning an operation or during an operation and is accepted in any operational state. If the CU is in the Inactive state (not busy) it responds by sending all zeros to the CPU via the BIN lines. If the CU is in any other state (busy) it responds by sending a 1 bit on BIN line 15; other lines are not significant but zeros.

3.13. SEND STATUS (SST).



Send Status (SST). This command is used to transfer the status word from the CU to the CPU. It is received in response to a program interrupt request (PII/) given when the CU is in the Wait Status state. The bits comprising the status word are listed in Table 3.2. The meaning of each bit, the status flip-flop concerned (in brackets under the meaning) and a brief description of possible reasons for a bit being set are also given.

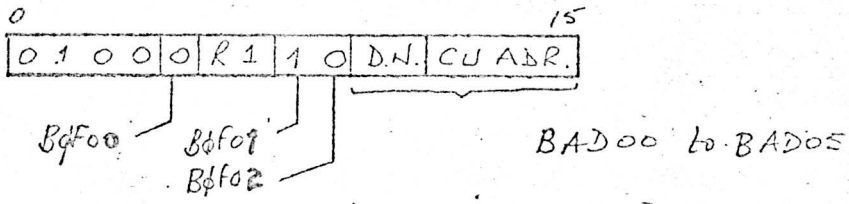
Table 3.2 P833 Cassette Tape CU Status Word. 7/2

BIN BIT	MEANING	DESCRIPTION
15	Not Operable; CU Busy. (FST15)	If set in response to an SST command, it indicates possible operator intervention required for one of the following reasons: no cassette in selected device; cassette unlocked (see paragraph 3.); no mains power. If set during a TST command it indicates that the CU is busy, or the addressed device rewinding
14	Throughput Error (FST14)	Set during a read or write operation if the Channel fails to reply to an exchange request (PIL/ or BRL/) within the required time. Data exchange is stopped, the interblock gap is realised and the CU switches to the Wait Status state.
13	Parity Error (FST13)	Set when a longitudinal parity error is detected by LRC logic during read-after-write or read operations. Data exchange is stopped only during the read operations.
12	Incorrect Length (FST12)	Set during a read operation when the tape block length differs from that given by the channel.
11	Program Error (FST11)	Set if an OTR is received from the channel when reading, an INR is received when writing or a wrong CIO START command is received. Data exchange is stopped.
10	Beginning or End of Tape (BET)	Indicates that the BOT or EOT marker hole has been detected during reverse or forward operations.

Table 3.2 Continued.

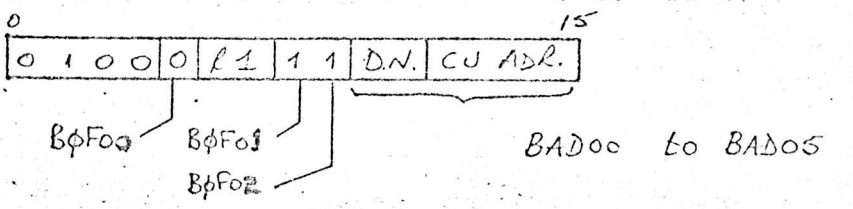
BIN BIT	MEANING	DESCRIPTION
9 8	Device Number (DA0; DA1)	These bits give the device number and are set during any SST command operation. Bit 8 is the most significant.
7	A or B Side (ANUM)	Indicates cassette A-side when set.
6	File Protect (WUN)	Set when any write operation is attempted on a file protected cassette (no Write Enable plug fitted). There can be no data exchange.
5	Not Used	Reserved. and nul
4	Not Used	Reserved. and nul
3	Tape Mark (FST03)	Indicates that a Tape Mark was sensed ~~on a Tape Mark format was detected with a data fault~~ during a read, space or search command.
2	Not Used	Reserved. and nul
1	Ready (FST01)	Indicates that a device has entered the ready state after being not ready (inoperable status; ~~tape rewind~~ condition).
0	Not Used	Reserved. and nul

3.14. CIØ STØP.



~~Main~~ STOP command. This command is accepted in any operational state and is used to stop data transfers between the CU and the CPU. It is normally programmed at the end of a data block to stop transfers on the Programmed Channel. The command does not affect the execution of Erase, Rewind or Space Block (Forward/Backward) operations.

3.15. CIO START.

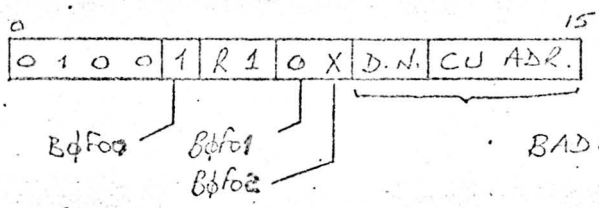


~~CIO START command~~. The CIØ START command code on the BØF lines is always accompanied by a cassette instruction on the BØU lines (see paragraph 3.26 and Table 3.3.). If the CU is in the Inactive state and the address is correct, the command is accepted and the operation defined by the cassette instruction commences. If the command is ~~not~~ assigned to an inoperable device (e.g. ~~no~~ no File Protect Plug, device Busy) it is ~~rejected~~ accepted if the CU is in the Inactive state. The CU switches to the Wait Status state, sends ~~SST~~ PIL/ and waits for the SST command.

Table 3.3 CIO Start Commands (Cassette Instructions).

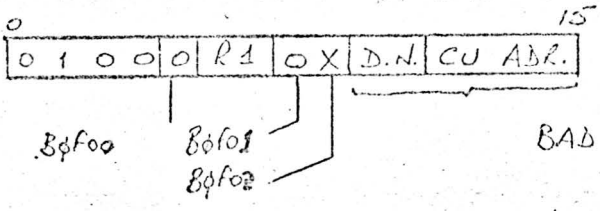
CODE (BOU) 12 13 14 15	NAME	DESCRIPTION
0 0 0 0	LOCK/UNLOCK	This command is used to lock or unlock the cassette in the addressed device and to put the heads in the end position (tape contact).
0 0 0 1	ERASE	This command is used to erase approximately 2.5 inches (6 cm) of the tape track in use. The command is normally used to erase a portion of tape that cannot reliably record data.
0 0 1 0	BACKSPACE ONE BLOCK	This command causes the tape to be moved in the reverse direction until an interblock gap is detected.
0 0 1 1	FORWARD SPACE ONE BLOCK	This command causes the tape to be moved forward to the next interblock gap.
0 1 0 1	WRITE ONE BLOCK	This command prepares the CU and the addressed device for recording data on tape. Data is transferred from the CPU using OTR commands.
0 1 1 1	READ ONE BLOCK	This command initiates a read data from tape operation. Tape movement is in the forward direction and data is transferred to the CPU using INR commands.
1 0 0 0	REWIND	This command causes the tape on the addressed device to be rewound at high speed to the Next ~~Beginning of~~ Tape hole.
1 0 1 1	SEARCH TAPE MARK FORWARD	The tape is moved forward to the interblock gap beyond the next Tape Mark on the track.
1 0 1 0	SEARCH TAPE MARK BACKWARD	The tape is moved ~~in the reverse~~ backward direction to the interblock gap beyond the next Tape Mark on the track, ~~to the Beginning of Tape Hole~~.

3.16. INPUT TRANSFER (INR)



INR command. This command is programmed when working on the Programmed Channel (no request required from the CU in inhibit mode) and simulated when working on the Multiplex Channel (Break Request, BRL/, required from CU). It is used during Read One Block operations (see paragraph 3.41) to transfer an 8-bit character from the CU to the CPU on the BIN lines. The command can only be accepted if the CU is in the Exchange state.

3.17. OUTPUT TRANSFER (OTR)



OTR command. This command is programmed when working on the Programmed Channel (no request required from the CU in inhibit mode) and simulated when working on the Multiplex Channel (BRL/ required from the CU). It is used during Write One Block operations (see paragraph 3.36) to transfer an 8-bit character from the CPU to the CU on the BOU lines. The command can only be accepted if the CU is in the Exchange state.

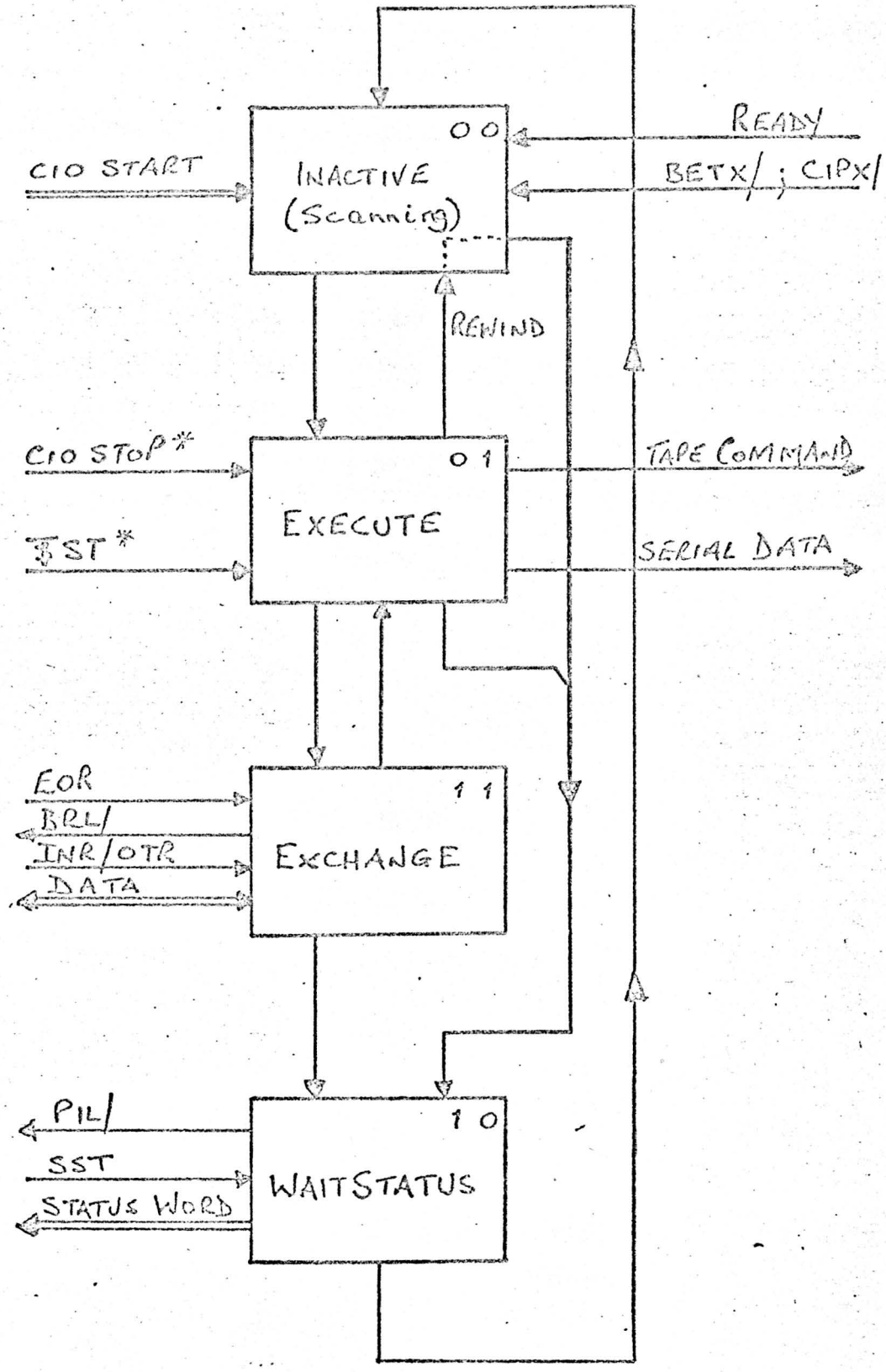
3.18 OPERATIONAL STATES

The P833 CU uses the four operational states common to all P855/P860/9 control units. These operational states are set by the two flip-flop sequensor, F0 - F1, which is controlled by the command code received from the CPU. Figure 3.3 shows the relationship between the states and the various data and control signals; the two-bit F-code is shown in each block.

3.19 INACTIVE (F0 - F1 = 0 - 0). In this state the CU is in standby mode waiting for a CIO START command (see paragraph 3.15). The CU scans the connected devices to test for operability and can check for the completion of a rewind operation (see paragraph 3.29) or a device becoming ready.

3.20 EXECUTE (F0 - F1 0 - 1). This state is used for the exchange of serial data (in 8-bit characters) and command information between the CU and the selected device. The CU switches to the Execute state on receipt of a valid CIO START command or after a valid OTR or INR command is received from the connected channel. When the operation is completed the CU normally switches to the Wait Status state (see paragraph 3.22). At the end of a Rewind operation, however, the CU returns to the Inactive state and can execute operations for devices other than that executing the rewind.

3.21 EXCHANGE (F0 - F1 = 1 - 1). This state is used for the exchange of parallel data (in 8-bit characters) between the CU and the CPU. The CU switches to the Exchange state at the start of every character serialization sequence during write operations, and at the end of every character deserialization sequence during read operations. The CU generates a transfer request (PIL/ or BRL/) and receives an INR or an OTR command from the channel. When the character is successfully transferred the CU returns to the Execute state, to read or write the next character, or goes to the Wait Status state if the block transfer is complete.



NOTE: These signals can be received in any operational state.

Figure 3.3. Operational States.

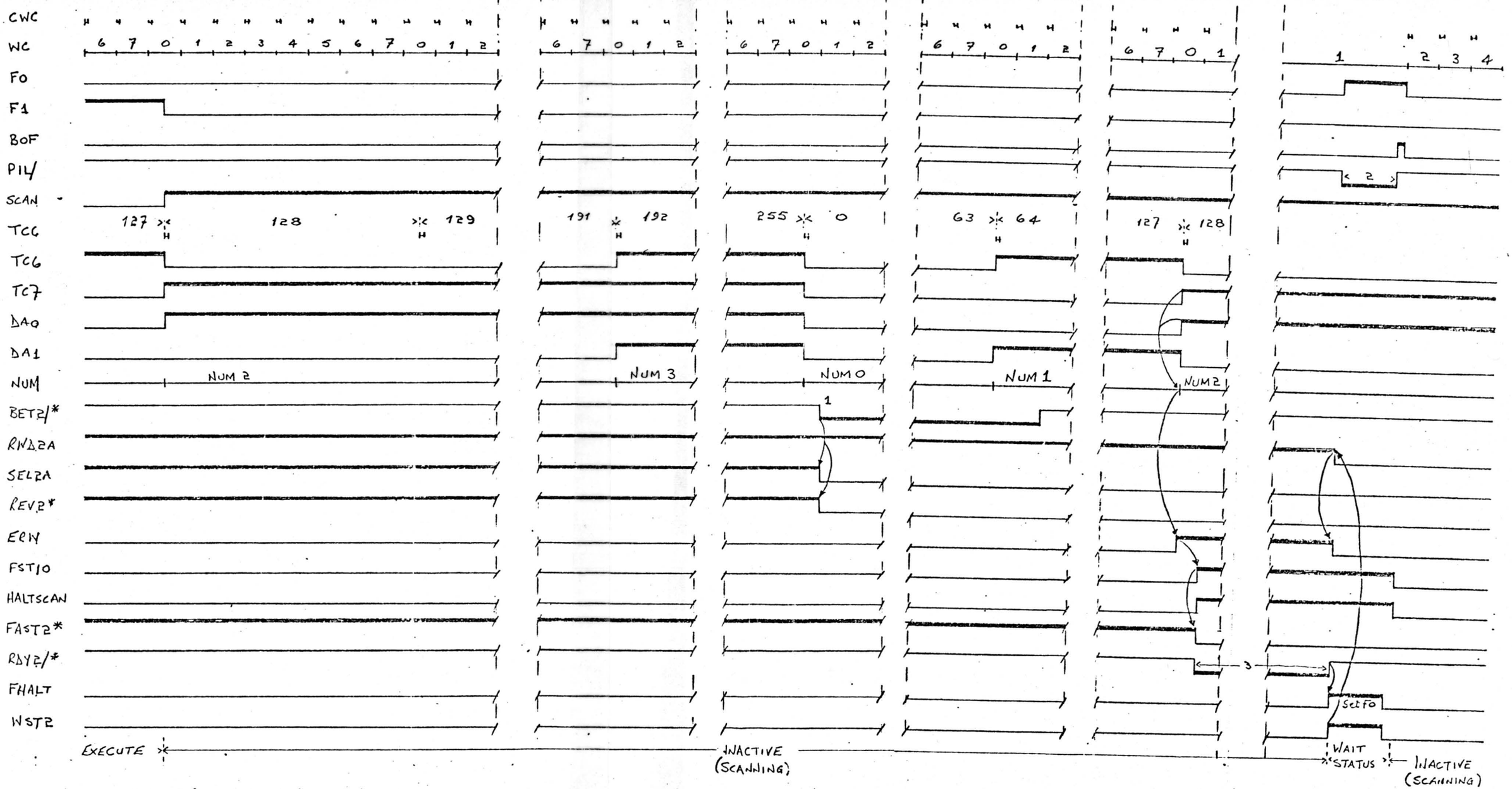
3.22 WAIT STATUS (F0 - F1 = 1 - 0). The CU is switched to this state at the end of a correctly executed operation (except Rewind), when a fault occurs or when a nonoperable device becomes operable. The interrupt request (PIL/) is sent to the CPU asking for an SST command. When this command is received the status word is sent to the CPU and the CU returns to the Inactive state.

3.23 SCANNING. In the Inactive state the CU scans the connected devices. The device number (DA0 and DA1) is incremented by the TC-counter (see paragraph 3.~~55~~) and every AP3RT time the current device is tested (ENDSCAN, Figure 3.~~25~~). If a change is detected the CU switches to the Wait Status state; if no change is detected the next device is tested.

3.24 The CU scan timing for the end of a Rewind operation detected on device number 2 is given in Figure 3.~~5~~. When flip-flop FST10 is set via ENDSCAN, the scanning operation is stopped and the FAST2* signal to the device is dropped. The device returns the RDY2/* signal (held low for 500 msec) and, when flip-flop FHALT is set, the ~~device~~ C.U. is switched to the Wait Status state (see ~~paragraph~~ paragraph 3.22). The subsequent ~~status~~ status word contains the device number and bit 10 is set.

3.25 If a new cassette (CIP/ signal) is detected ~~or~~ and a device becomes Ready (RDY/ signal), flip-flop FST01 is set to set flip-flop FHALT. The subsequent status word gives the device number with bit 1 set.

3.26 CASSETTE INSTRUCTIONS. The cassette instructions are extensions of the CIO START command and are transferred from the CPU on BOU12 to BOU15. When a CIO START command is received, the code on the BOU lines is clocked into the Function flip-flops (Figure 3.26, FCT) which set up the CU for the operation to be performed. Table 3.3 lists the instructions used, gives the BOU line codes and gives a brief description of each instruction.



NOTES: 1. End of Rewind detected on device no 2.

2. Time dependent on central processor.

3. Waiting time for RDY2/* to return high is 500msecs.

Figure 3.5. SCAN TIMING.

3.27 CIO LOCK/UNLOCK. This command is used to lock or unlock a cassette in a device. It also positions the heads, moving them to the tape contact position. Timing is shown in Figure 3.6.

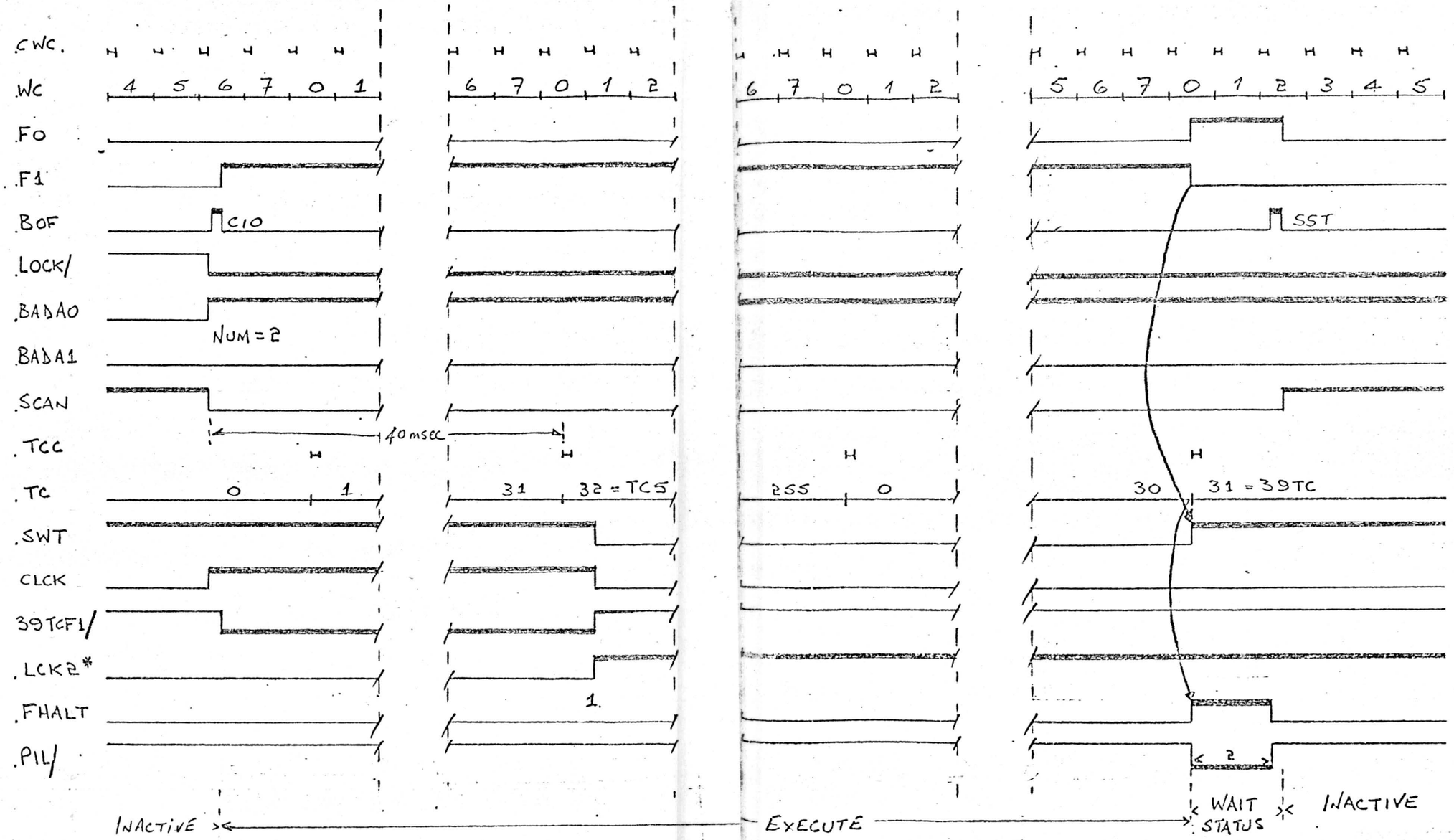
Run on

When the command is accepted the CU switches to the Execute state and, after the start delay, the addressed device is selected and LCKX* is sent to the device. At the next 39TC time the FHALT flip-flop is set switching the CU to Wait Status. The subsequent status word contains the device number.

3.28 If a CIO command other than CIO Lock/Unlock or CIO Rewind is attempted on an unlocked device, the CU accepts the command and goes to the Wait Status state. The subsequent status word contains the device number and bit 15 is set.

3.29 CIO REWIND. This command must be programmed when starting a job on a track which is not at the Beginning of Tape (BET) hole. The tape on the addressed device is rewound at high speed to the BET hole. Rewind timing is shown in Figure 3.7. When the command is accepted the CU switches to the Execute state and, after the start delay, selects the addressed device. The FASTX* and REV* signals are sent to the device. At the next TC7 time (130 msec. later) ~~the FHALT flip-flop is set, switching~~ the CU back into the Inactive state.

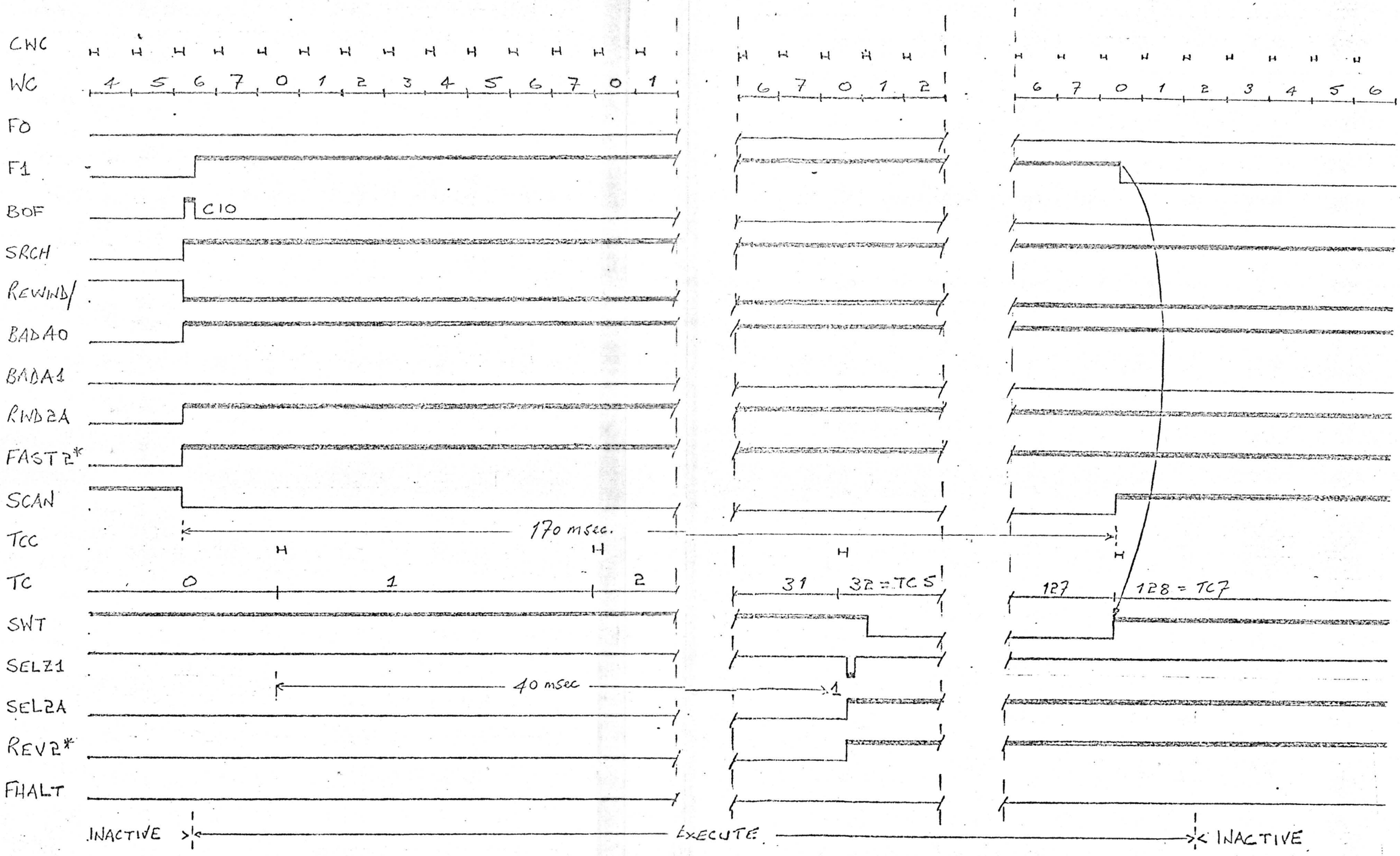
3.30 The maximum rewind time is 45 seconds and when the tape reaches the BET hole the condition is detected. If the BETX/* SIGNAL IS RECEIVED FROM THE DEVICE DURING THE Rewind command operation time, the tape does not stop at the BET hole. The CU switches to the Inactive state at the end of the command execution time, the



NOTES: 1. Select addressed cassette unit (Nr. 2).

2. Time dependent on central processor.

Figure. 3.6. LOCK/UNLOCK TIMING



NOTES: 1. Select addressed cassette unit (Nr. 2).

Figure 3.7. REWIND TIMING.

Rewind condition is detected as explained in paragraph 3.[illegible] and the CU goes to the Wait Status state. The subsequent status word contains the device number and bit 10 is set.

3.31 ERASE. This command is a dummy write operation and is used to erase a 256 character block length (approximately 6.5 cm) on the selected track. Timing is shown in Figure 3.[illegible]. When the command is accepted the CU switches to the Execute state and after the start delay, selects the addressed device. The Write (WCDX*) and Forward (FWDX*) signals are sent to the device but the write flip-flop is not set. At the next TC39 time FHALT is set and FWDX* is dropped. The CU goes to the Wait Status state at TC7 time, WCDX* is dropped and the Program Interrupt is sent to the CPU. The subsequent status word gives the device number and, if the End of Tape area was detected during the operation, bit 10 is set.

3.32 Space One Block (Forward/Backward). The space block commands are used to move the tape in the required direction to the next interblock gap on the selected track. Timing is shown in Figure 3.9. When the command is accepted the CU switches to the Execute state and selects the addressed device after the start delay. The required direction signal (FWDX* or REVX*) is sent to the device at TC5 time and the read signal (RCDX*) is sent at RTC time. The device reads a data block (see paragraph 3.41.) and the CU deserializes the data but does not check the LRC. No data exchange occurs with the CPU. The device stops when the next interbloxk gap is detected. The read signal is dropped at the end of the block and FHALT is set at the following 39TC time. The CU switches to the Wait Status state and sends PIL/ to the CPU.

3.33 The subsequent status word sent to the CPU gives the device number. If a Tape Mark is detected bit 3 is set; if the End or Beginning of Tape indication is detected bit 10 is set. If the operation is performed on a blank track (no previously recorded data on the track) the tape is moved (forward or backward) to the end of the tape and no interrupt is sent to the CPU.

3.34 SEARCH TAPE MARK(FORWARD/BACKWARD). Search commands are used for Tape Mark detection on the selected track. Timing is shown in Figure 3.10. When the command is accepted the CU switches to the Execute state and selects the addressed device (sends the FWDX* or REVX* signal) after the 22 μsec start delay. At RTC time the read signal (RCDX*) is sent to the device and the read flip-flop (SRA) is set. The device reads data from tape (see paragraph 3.41) and the CU de-serializes the data but does not check the LRC (see paragraph 3.54) There is no data exchange with the CPU. The device stops at the interblock gap after a Tape Mark is recognised and FST03 is set. At the next 39TC time FHALT is set and the CU switches to the Wait Status state and sends PIL to the CPU.

3.35 The status word sent to the CPU gives the device number and bit 3 (Tape Mark) is set. If the operation is performed on a blank track (no previously recorded data on the track) the tape is moved (forward or backward) to the end of the tape and no interrupt is sent to the CPU.

3.36 Write One Block. This command prepares the CU and the selected device for recording a block of data on tape. After the command is accepted, it is followed by OTR commands which are received in response to Program Interrupts (PIL/) or Break Requests (BRL/) given by the CU. Data transfer is stopped by either a CIO HALT command or an End of Range (EOR) signal.

3.37 Figure 3.11 shows the timing for a typical block transfer. When the command is accepted the CU switches to the Execute state and sends the Write signal (WCDX*) to the selected device. After the start delay, (~~about 10 msec~~), the addressed device is selected (FWDX* is sent) and ~~approximately 16 msec later~~ (at RTC time) the read flip-flop (SRA) is set. When the TC-counter reaches TC7, and the Write Bit Counter (WC-register, see paragraph 3.51) is at 1WC/, the Preamble character is loaded into the Write Serializer. Flip-flops FREAD and SWA are set and the TC-counter is stopped. The CU switches to the Exchange state and sends a Break Request (BRL/) on the Multiplex channel. The Preamble character is serialized and sent to the selected device on the WDL line.

3.38 When the OTR command is received from Multiplex, the data character on the BOU lines is loaded into the CB-register. The CU switches to the Execute state and, when serialization of the previous character is finished, WSR is again loaded by 1WC/. At this time FREAD is again set, switching the CU back into the Exchange state and BRL/ is sent to the Multiplex. The data transfer continues in this manner, with the CU in the Exchange state to receive characters from the Multiplex and in the Execute state to serialize the characters and send them to the selected device. The last character received is the LRC character.

3.39 All characters are read back approximately 20 msec (read head to write head gap) after the Preamble character is written on tape. Reading back the data resets the TC-counter to zero. The characters are deserialized by the RLR-register (see paragraph 3.54) to perform a read-after-write LRC error check. When a CIO HALT command, or EOR from the Multiplex is received, Break Requests are inhibited and the Postamble is serialized and sent to the device. When the read-after-write operation ends, 20 msec after the Postamble is written, the TC-counter is started and the 85 msec write stop delay begins.

3.40 At TC6 time flip-flop FHALT is set and FWDX* to the device is dropped. The CU waits a further 85 msec before switching to the Wait Status state to ensure that the device is stopped. The CU sends PIL/ to the CPU and receives an SST command in reply. The subsequent status word gives the device number and if a data error occurred during the transfer, bit 13 gives the Parity Error indication.

3.41 READ ONE BLOCK. This command is used to read data from tape. After the command is accepted it is followed by INR commands which are received in response to Program Interrupts (PIL/) or Break Requests (BRL/) given by the CU. Data transfer is stopped either by a CIO HALT command or an EOR signal from the Multiplex.

3.42 Figure 3.11 shows the timing for a typical Read One Block operation. When the command is accepted the CU switches to the Execute state. The addressed device is selected at the end of the start delay (FWDX* is sent at TC5 time) and about 16 msec later (during RTC time) flip-flop SRA is set. This stops the TC-counter and the Read signal (RCDX*) is sent to the device. The CU waits for the device to transfer serial data on the RDAX/* line.

3.43 When data is received from the device, the Read Circuit (see paragraph 3.62) is started and the TC-counter is reset to zero. The data received is deserialised by the Read Deserializer (see paragraph 3.52) and made available to the CB-register. The RC-counter (see paragraph 3.53) resets flip-flop FENDA at the end of the Preamble character and 7RC produces CWCR/ to clock the WC-counter. At the end of subsequent data characters, 7RC produces STRR/ which loads the CB-register and sets flip-flop FREAD. The CU switches to the Exchange state and generates a BRL/ signal which results in an INR command being received from the Multiplex.

3.44 When the INR command is received, the data character in the CB-register is loaded into BINL and BINR and put on the BIN lines to the Multiplex. The CU returns to the Execute state to process the next character and data transfer continues as described above. The data read is also processed by the RLR-register (see paragraph 3.54) and if a data error has occurred flip-flop FST13 is set by MP at the end of Postamble deserialization.

MAIN LOGIC ELEMENTS.

3.45 REGISTERS.

The P833 Cassette Tape CU contains 14 main registers, counters and decoder plus the Selection logic, which control the instruction operations and the data flow. In the following descriptions these are roughly grouped into those elements concerned primarily with data flow, those concerned with timing and delay functions and those concerned with I/O commands and cassette instructions. The elements concerned with device selection are grouped under a single heading. All the elements described are shown in the logic diagrams (figures 3.25, 3.26 and 3.27) at the end of this section.

3.46 CBD-Selector: Two quad 2-input multiplexers which are are controlled by READ/. It selects either write data from BOU08 to 15 or read data from the Read Deserializer (RSR). The output is fed to the CB-register.

3.47 CB-Register. This is the main data buffer in the CU. During write operations data from the BOU lines (via CBD) is clocked into the register by ACOTR/. During read operations the register is loaded by STRR/. The output is either to the BIN lines (via BINL and BINR) or to the Write Serializer (via WSRD).

3.48 BINL and BINR Selectors. These are quad 2-input multiplexers which load either read data from the CB-register, or status information, onto the BIN lines to the CPU. The selection is controlled by BINE/ (ACSST + ACINR) and WST.

3.49. WSRD-Selector. These are quad 2-input multiplexers which are controlled by FENDA and whose output load the Write Serializer (WSR). The Preamble/ Postamble character $(01010101)_2$ is hard-wired on one set of the inputs. At the beginning or end of a write operation (see paragraph 3.36) when FENDA is high.....

TYPIST!!! Continue on next page

this character is loaded into the Write Serializer (WSR). During the remainder of the operation, the data characters received from the CB-register are loaded into WSR (FENDA is low).

3.50 Write Serializer (WSR). The Write Serializer comprises two 4-bit shift registers cascaded to form an 8-bit shift register. Parallel input information (one 8-bit character) is loaded into the register (see paragraph 3.37) by 1WC/ and the register is clocked by AP3RT. The serial output is exclusive-ORed with ORT and 2RT (Hyphase and Bit times) and the result controls the write data flip-flop WDL.

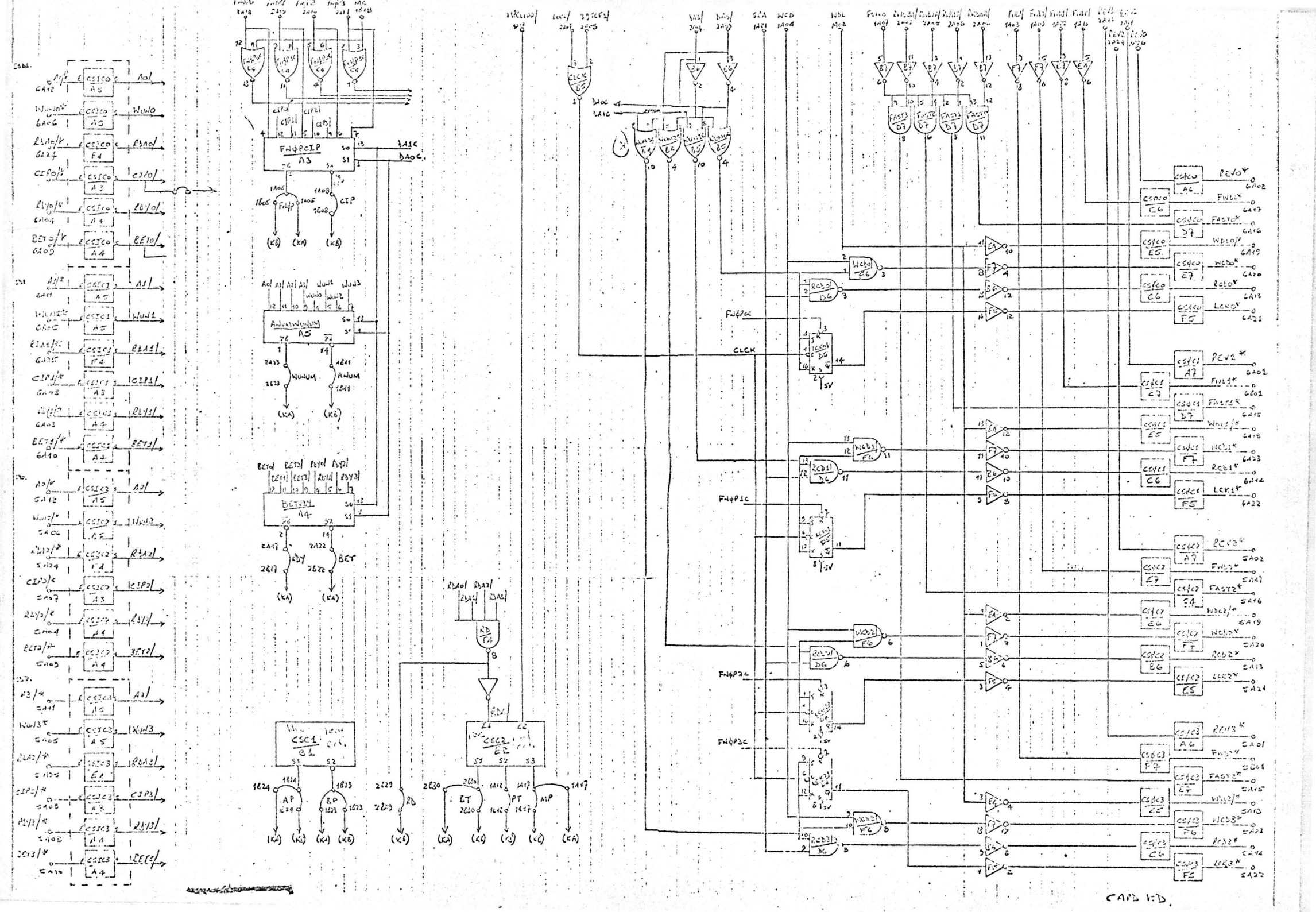
3.51 WC-Register. This is a 4-bit binary counter whose outputs are decoded by 0145WC. The counter is controlled by the WCPE/ and WCEP signals, which both must be high to enable the count mode, and is clocked by the CWC pulses (CWC = CWCR/+CWCW/) at BP.2RT time. Together with 0145WC, the WC-register forms a bit counter during write operations and is clocked once per bit by CWCW/. During read operations the WC-register is clocked by CWCR/ and forms a byte counter with 0145WC.

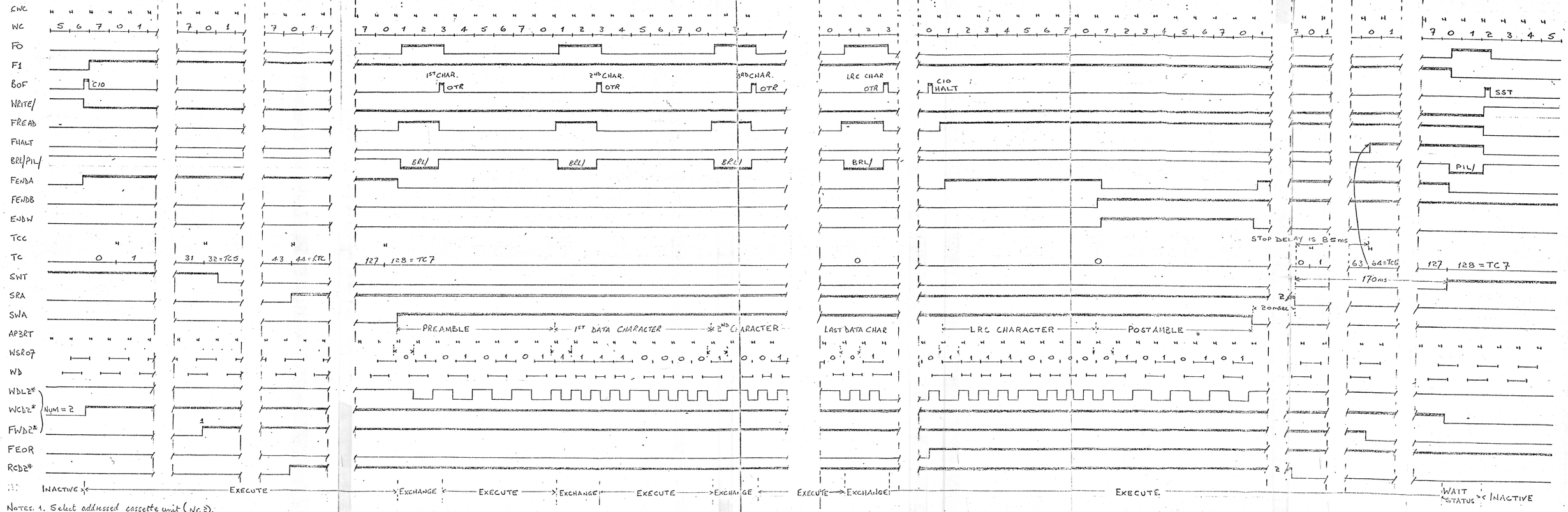
3.52 Read Deserializer (RSR). The Read Deserializer comprises two 4-bit shift registers cascaded to form an 8-bit shift register. The Shift registers have J-K inputs which are tied together to give D-type entry characteristics. (the register is reset at the end of each data packet) The serial data (RD) is shifted right by the BT clock pulses from the Read Circuit (see paragraph 3.62) The output is taken in parallel form and loaded into the CB-register (via CBD) by the STRR/ pulses.

3.53 RC-~~Register~~ Counter. This is a 4-bit binary counter which is controlled by the READ signal and clocked by the PT pulses from the Read Circuit (see paragraph 3.62). During read operations the decoded outputs produce 7RC (at the end of every 8-bit character) which enables STRR/, and the character from the Read ~~Serializer~~ Deserializer is loaded into the ~~CBX~~ CB-register.

3.54 RLR-Register. This register is identical to the Read Deserializer and is used to detect errors in the LRC character. The data received serially from tape is exclusive-ORed with the most significant bit of the RLR-register. RLRX is produced ~~which~~ and is shifted through the register by BT. Parallel outputs from the register are decoded to give ORLR/. When the LRC character is shifted into the register, the contents should be all zeros and ORLR/ should be low. If ORLR/ is high, a data error has occurred and results in bit 13 of the subsequent status word being set (FST13Z1/ = TRANS. MP. ORLR/) to give the Parity Error ~~Error~~ indication to the CPU.

3.55 TC-Counter: ~~This comprises~~ Two 4-bit binary counters cascaded to form an 8-bit counter whose decoded outputs provide the necessary start, stop, read and write delays required by the cassette tape subsystem. The counter is incremented once per character by TCC (TCC/= BP.ORTA.TCE. OWC) and has, therefore, a period of 1.333 msec. It is reset to zero when a CIO START command is accepted and when data is read from tape (TCMR = ACIO + BT). Table 3.4 gives the TC-counter bit settings which correspond to the various delays. During Scanning (see paragraph 3.73) the tape number is incremented by TC6 and TC7.


CARD H:D.



Notes. 1. Select addressed cassette unit (Nr. 2).
2. These signals drop after the "End-of-tape-write" operation (Unload and 2 in Postamble)

Figur 3.11. WRITE ONE BLOCK TIMING.

Table 3.4 Pre-record and Post-record Time Delays.

TC BITS 7 6 5 4 3 2 1 0	SIGNAL	TIME (msec)	NAME
0 0 0 1 1 1 1 1	39TC	41.3	Normal stop delay
0 0 1 0 0 0 0 0	~~40~~ TC5	42.6	Start delay.
0 0 1 0 1 1 0 0	RTC	58.6	Start read delay.
0 1 0 0 0 0 0 0	TC6	85.3	Write stop delay.
1 0 0 0 0 0 0 0	TC7	170.6	~~Write stop~~ Start write delay.

NOTE: The times given above ~~are exact but the actual times may be slightly less~~ may be decreased by up to 1.33ms due to the asynchronous nature of CIO commands and the start and end of read data signals.

3.56 Clock Logic. The clock circuit comprises two interconnected D-type flip-flops which are strobed by the AP and BP pulses from the Write Circuit. The ORT to 3RT pulses are produced which are used in conjunction with the AP and BP pulses to provide the general timing requirements of the CU. Figure 3.4 gives the clock pulse timing.

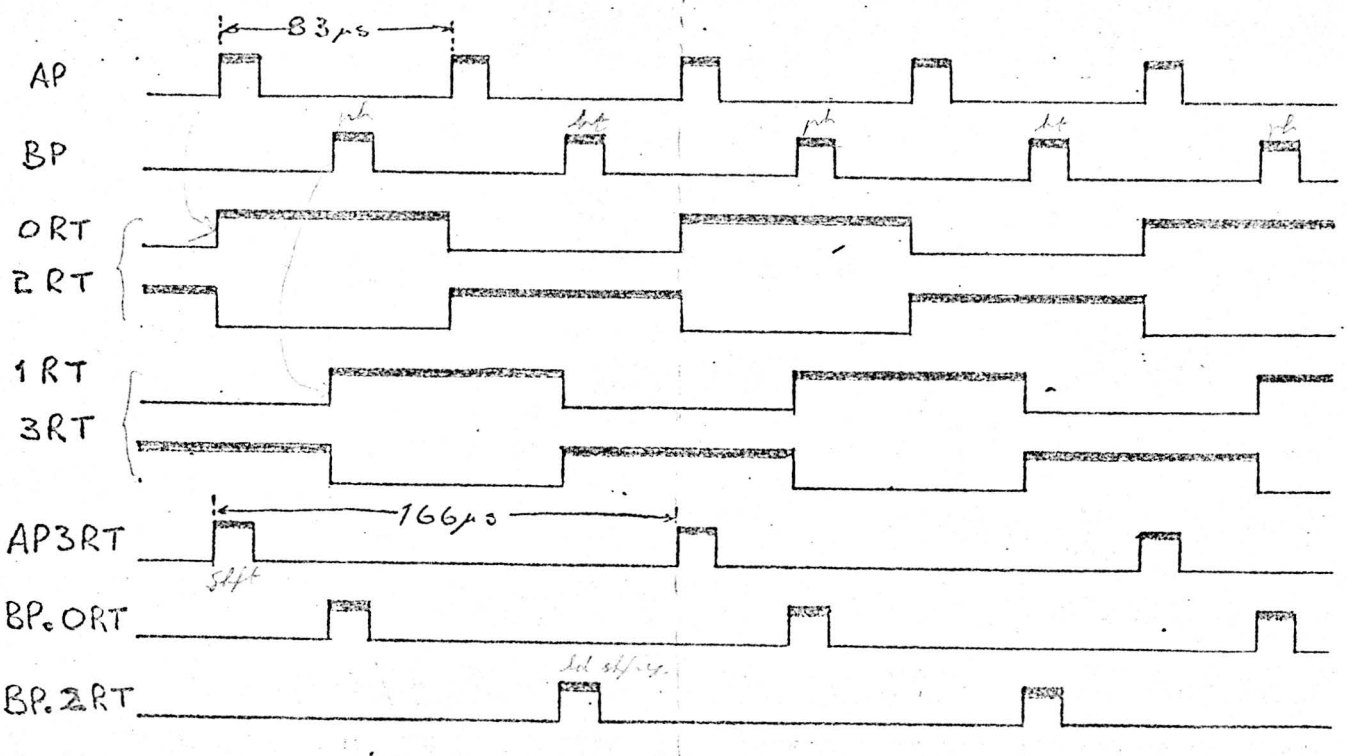


Figure 3.4 Clock Pulse Timing.

3.57 Command Decoder (COMMAND) This is a 1-of-10 decoder used to decode the received I/O command on the ROF lines. Provided the CU address is correct (AREA must be low) the appropriate low ouput is produced.

3.58 Function Decoder (FCT). This comprises four D-type flip-flops which are set according to the cassette instruction code on BOU12 to 15. The flip-flops are clocked by ACIOB when a CIO START command is accepted.

3.59 CIO Decoder. This is a 1 of 10 decoder used to decode the state of the Function Decoder flip-flops. It gives a low output appropriate to the cassette instruction to be executed.

3.60 Selection Logic. The Selection logic comprises a number of flip-flops, gates and selectors elements which produce signals for device control the device being selected according to the device number. The device number is given by DA0 and DA1 which are decoded to produce NUM0 to NUM3 and NUM0C to NUM3C. NUM0 to NUM3 are used to select the appropriate Rewind (RWDXA), Reverse (REVX), Forward (FWDX) and Not Operable (FNOPX) signals. NUM0C to NUM3C are used to select the appropriate Write (WCDX), Read (RCDX) or Lock (LCKX) signal as required. DA0 and DA1 are also used during scanning (see paragraph 3.23). An input control signal from a device is not recognised by the CU unless the device number corresponds to that given by DA0 and DA1.

3.61 Write Circuit. This is a special circuit (see paragraph 3.70) which provides timing pulses for write operations. The circuit is basically an oscillator with a base frequency of 6.144 KHz which, after suitable division and decoding, provides the AP and BP timing pulses.

3.62 Read Circuit. This is a special circuit (see paragraph 3.71) whic is driven by the data bits read from tape. The circuit provides the BT and PT timing pulses used during any read operation. The MP signal detects interblock gaps sets and resets the SRA flip-flop at the ~~standard~~ end of an operation and is instrumental in status bit setting for the Tape Mark, Incorrect Length and Parity Error indications.

3.63 CONTROL FLIP-FLOPS

The following table lists and describes the most important flip-flops in the CU.

Mnemonic	Description
FENDA	End of serialization flip-flop; enables serialization of Preamble and Postamble characters during write operations.
FENDB	End of deserialization flip-flop; stops Preamble and Postamble characters being sent to the CPU during read operations.
FEOR	End of range flip-flop; synchronizes EOR signal or a CIO STOP command. When set data transfer is stopped and the Postamble character is serialized when writing.
FHALT	Stop condition flip-flop; set at the end of a correctly executed operation or if a fault occurs during an operation. The CU switches to Wait Status.
FNOP0 - FNOP3	Device not operable flip-flops. Set when the corresponding device is not operable; reset when the CU goes to Wait Status or the device becomes ready.
FREAD	Initiate Break Request (BRL/) flip-flop. Set during data transfers by STR pulses; reset when an OTR or an INR command is received. This allows use of BRL at the leading edge of OTR/STR instead of trailing edge for FO.
FWD	A Function flip-flop; set by BOU15 and indicates tape direction.
F0 - F1	Two flip-flop sequensor (see paragraph 3.18).

3.64 INTERFACE SIGNALS. The following signal list contains the significant interface signals related to the P833 CU. The signals are grouped according to whether they are related to the CPU or a device. Signals related to the cassette drives are indexed in text and on drawings by 0,1,2 and 3. However, in this list they are indexed by X as it is considered unnecessary to quadruplicate the information. Signals within the CU are not listed here but are included in text and on the logic drawings.

CPU Interface Signals

Signal	Meaning
BAD00/ to BAD01/	Device address lines.
BAD02/ to BAD05/	Control unit address lines.
DAV/	~~Device Address~~ Interface DAta Validation line.
BOF00/ to BOF02/	I/O command lines.
[illegible]	[illegible]
BOU08 to BOU15	Cassette instruction and data out lines from CPU.
ACC/	Command accepted.
ARE/	Address recognised.
PIL/	Program interrupt.
BRL/	Break request.
EOR	End of Range signal.
MC/	Master Clear.
BIN00/, BIN03/, BIN06/ to BIN15/	Data in and status lines to CPU.

Device Interface Signals

CU to Device

Signal	Meaning
REVX*	Reverse tape motion indicator.
FWDX*	Forward tape motion.
FASTX*	With REVX' indicates fast rewind.
WDLX/*	Write Data line.
WCDX*	Write command.
RCDX*	Read command.
LCKX*	Lock or Unlock.

Device to CU

Signal	Meaning
AX/*	Cassette A side or B side.
WUNX*	File Protect indication.
RDAX/*	Read data line.
CIPX/*	Cassette in place indication.
RDYX/*	Device Ready.
BETX/*	Beginning or End of Tape.

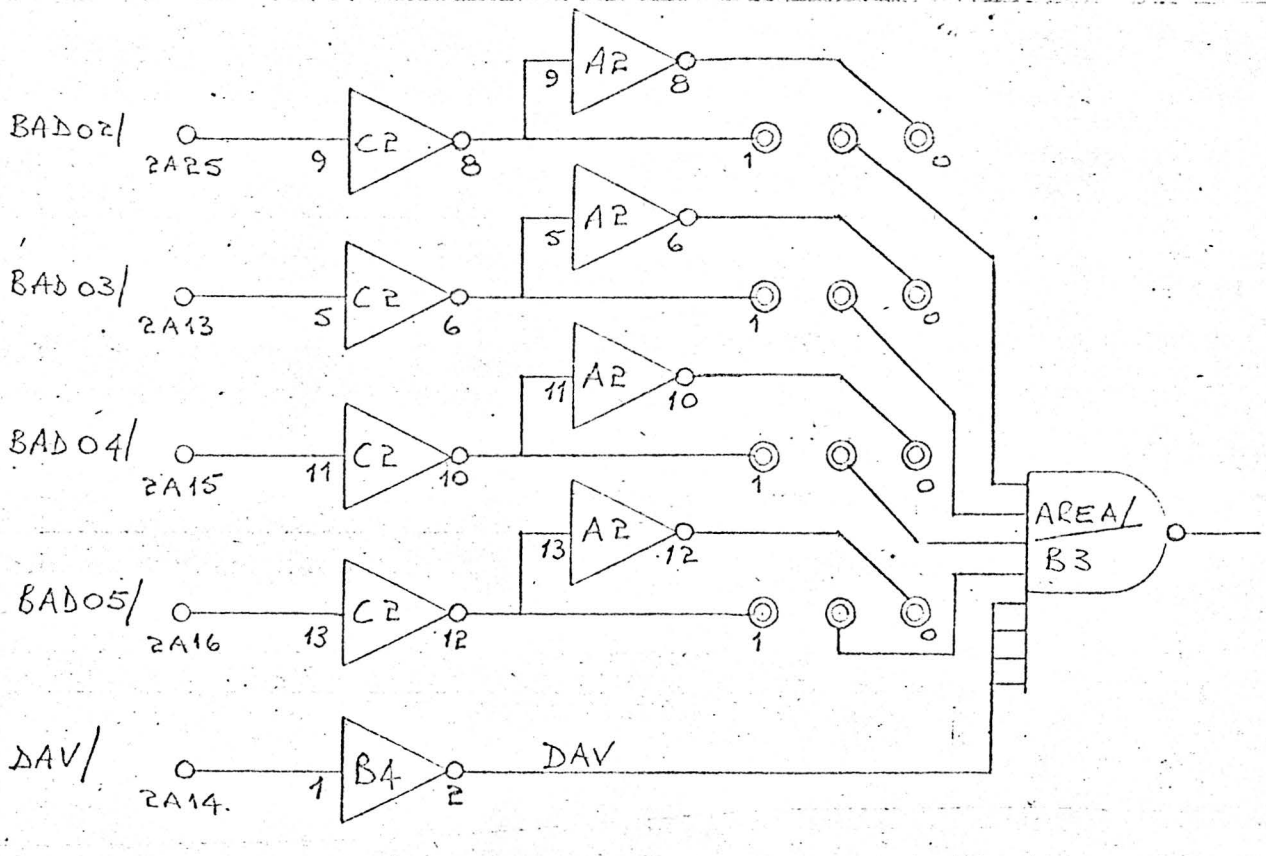
3.65 PHYSICAL AND INTERCONNECTIONS

The P833 cassette tape ~~unit~~ CU comprises three printed circuit cards mounted in a standard 5-card rack along with an I/O Extender card (IORC) and the power supply modules. See Figure 3.14 . The I/O Extender card is described in Section I of this manual and modular power supply information is included as Appendix B of the manual.

3.66 PRINTED CIRCUIT CARDS. The CU logic is contained on standard P855/P860 logic cards. The CU cards are called KA, KB and KD; their relative mounting positions are shown in Figure 3.14 and card layout is shown in Figures 3.17 to 3.19.

3.67 INTERCONNECTIONS. General cabling information and connections is given in Figure 3.15 . I/O cabling information between the 5-card rack and the CPU is given in Section I. Table 3.5 lists the connections between the IORC card and the CU cards; Table 3.6 lists the CU card interconnections; Tables 3.7 and 3.8 give cabling information between the CU and up to four cassette tape drives.

3.68 CU ADDRESS AND CHANNEL STRAPS. The CU address code and the channel must be set by wiring straps on card KB (see Figure 3.18) prior to or during system installation. The address logic involved and an example address strapped is shown in Figure 3.16 . The CU is working on the Multiplex Channel in the example.



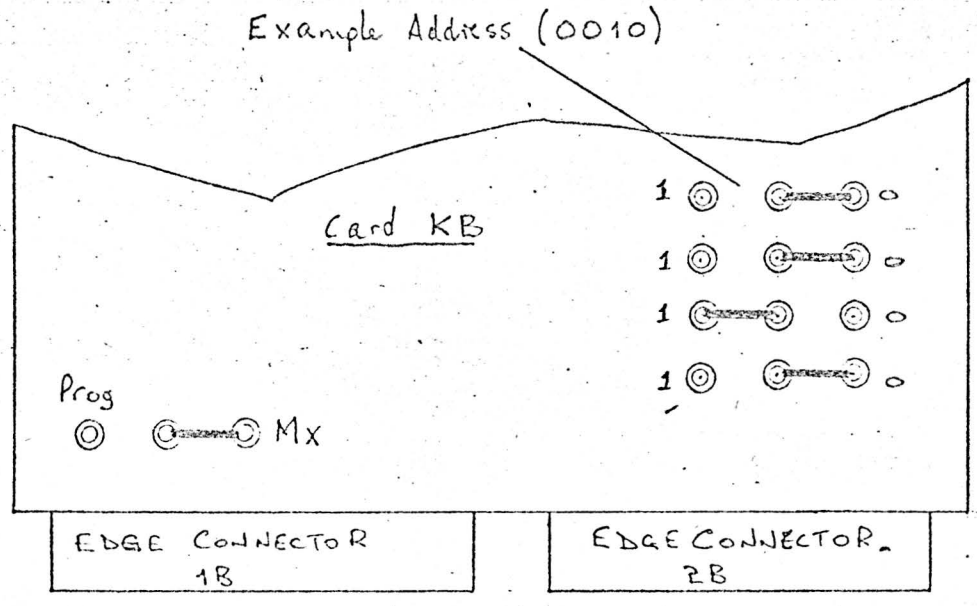


Figure 3.16 CU Address And Channel Stepping.

Table 3.5 I/O Card ~~Cabling~~ Connections

Signal	I/O Pin Nr.	Card KB Pin Nr.	Signal	I/O Pin Nr.	Card KB Pin Nr.
BADO0/	2A22	2A22	BOU13	2B06	2A06
BADO1/	2A24	2A24	BOU14	2B05	2A05
BADO2/	2A25	2A25	BOU15	2B11	2A11
BADO3/	2A13	2A13	DAV/	2B14	2A14
BADO4/	2A15	2A15	EOR	2B02	2A02
BADO5/	2A16	2A16	MC/	2B12	2A12
BOFO0/	2A04	2A04			
BOFO1/	2A03	2A03	ACC/	1B13	1A13
BOFO2/	2A01	2A01	ARE/	1B14	1A14
BOUO0	2A28	2A28	BINO1/	1B04	1A04
BOUO1	2A27	2A27	BINO3/	1B06	1A06
BOUO2	2A26	2A26	BINO6/	1B09	1A09
BOUO3	2B23	2A23	BINO7/	1B10	1A10
BOUO4	2B21	2A21	BINO8/	1B21	1A21
BOUO5	2B20	2A20	BINO9/	1B28	1A28
BOUO6	2B19	2A19	BIN10/	1B29	1A29
BOUO7	2B18	2A18	BIN11/	1B30	1A30
BOUO8	2B17	2A17	BIN12.	1B31	1A31
BOUO9	2B08	2A08	BIN13/	1B26	1A26
BOU10	2B09	2A09	BIN14/	1B22	1A22
BOU11	2B10	2A10	BIN15/	1B27	1A27
BOU12	2B07	2A07	BRL/	1B16	1A16
			PIL/	1B15	1A15

Table 3.6 Russum card [illegible]-connections.

Signal	Card KA Pin Nr.	Card KB Pin Nr.	Card KD Pin Nr.
ACINR/	2A19	2B19	
ACIO	2A24	2B24	
ACOTR/	2A14	2B14	
AP3RT	2A13	2B13	
AREA/	2A16	2B16	
BADA0	2A26	2B26	
BADA1	2A27	2B27	
CWCR/	2A08	2B08	
ENDW/	1A14	1B14	
FEORZ1/	2A25	2B25	
FSTO1Z1/	1A09	1B09	
FSTO1	1A06	1B06	
FWD	1A31	1B31	
READ	2A01	2B01	
SCAN	2A03	2B03	
SRCH	2A02	2B02	
SST/	2A15	2B15	
STR	2A28	2B28	
TRANS	1A30	1B30	
2RT	2A06	2B06	
ACSST	1A04	1B04	
CLOCK FO/	2A18	2B18	
DA0	1A21	1B21	
DA1	1A16	1B16	
ENDSCAN	1A13	1B13	
FEOR	2A23	2B23	
FHALT	2A20	2B20	
FST 10Z1/	1A29	1B29	
FST 15Z1/	1A26	1B26	

Table 3.6 Continued.

Signal	Card KA Pin Nr.	Card KB Pin Nr.	Card KD Pin Nr.
FO/	2A17	2B17	
F1/	2A21	2B21	
INIBRA/	2A22	2B22	
READC/	1A02	1A02	
RWDOA	2A12	2B12	
RWD1A	2A11	2B11	
RWD2A	2A10	2B10	
RDWD3A	2A09	2B09	
SWA	1A27	1B27	
WRONGCIO/	2A05	2B05	
WST	1A22	1B22	
WUN	1A10	1B10	
1WC/	2A04	2B04	
4WC	1A28	1B28	
ANUM		1B11	1B11
AP	1B24	1B24	1B24
BP	1B23	1B23	1B23
CIP		1B08	1A08
FNOP	1A05	1B05	1A05
MP	1A17	1B17	1A17
PT		1B12	1A12
BT	2A30	2B30	2B30
RD		2B29	2B29
WDL		1B02	1A02
FSTIO	1A07	1B07	1A07
MC	1A18	1B18	1B18
BETO/	2B16		2A16
BET1/	2B14		2A14
BET2/	2B12		2A12
BET3/	2B10		2A10

Table 3.6 Continued.

Signal	Card KA Pin Nr.	Card KB Pin Nr.	Card KD Pin Nr.
BET	2B17		2A17
CIPO/	2B15		2A15
CIP1/	2B13		2A13
CIP2/	2B11		2A11
CIP3/	2B09		2A09
RDY	2B22		2A22
WUNUM	2B23		2A23
DAO/	2B03		2A03
DA1/	2B04		2A04
FNOPO	2B18		2A18
FNOP1	2B19		2A19
FNOP2	2B20		2A20
FNOP3	2B21		2A21
FWDO/	1B10		1A10
FWD1/	1B22		1A22
FWD2/	1A08		1A09
FWD3/	1B03		1A03
LOCK/	2B07		2A07
MP CLEAR/	1A19		1A18
REVO	2B26		2A26
REV1	2B27		2A27
REV2	2B24		2A24
REV3	2B25		2A25
RWDOA/	2B02		2A02
RWD1A/	2B06		2A06
RWD2A/	2B05		2A05
RDW3A/	2B01		2A01
SRA	1B21		1A21
WCD	1B04		1A04
39TC FA/	2B08		2A08

Table 3.7. Cable Connections CU to Device Nrs. 0 And 1.

Signal	Card KD Pin Nr.	Cable J2 Pin Nr.	Signal	Card KD Pin Nr.	Cable J2 Pin Nr.
WUN0*	6A06	1	FAST0*	6A15	14
WUN1*	6A05	2	LCK0*	6A21	15
BET0/*	6A09	3	LCK1*	6A22	16
BET1/*	6A10	4	CIP0/*	6A07	17
RCD0*	6A13	5	CIP1/*	6A08	34
RCD1*	6A14	6	RDY0/*	6A04	35
WCD0*	6A20	7	RDY1/*	6A03	36
WCD1*	6A23	8	A0/*	6A12	37
RDA0/*	6A24	9	A1/*	6A11	38
RDA1/*	6A25	10	REV0*	6A02	39
WDL0/*	6A19	11	REV1*	6A01	40
WDL1/*	6A18	12	FWD0*	6A17	41
FAST0*	6A16	13	FWD1*	6B01	42

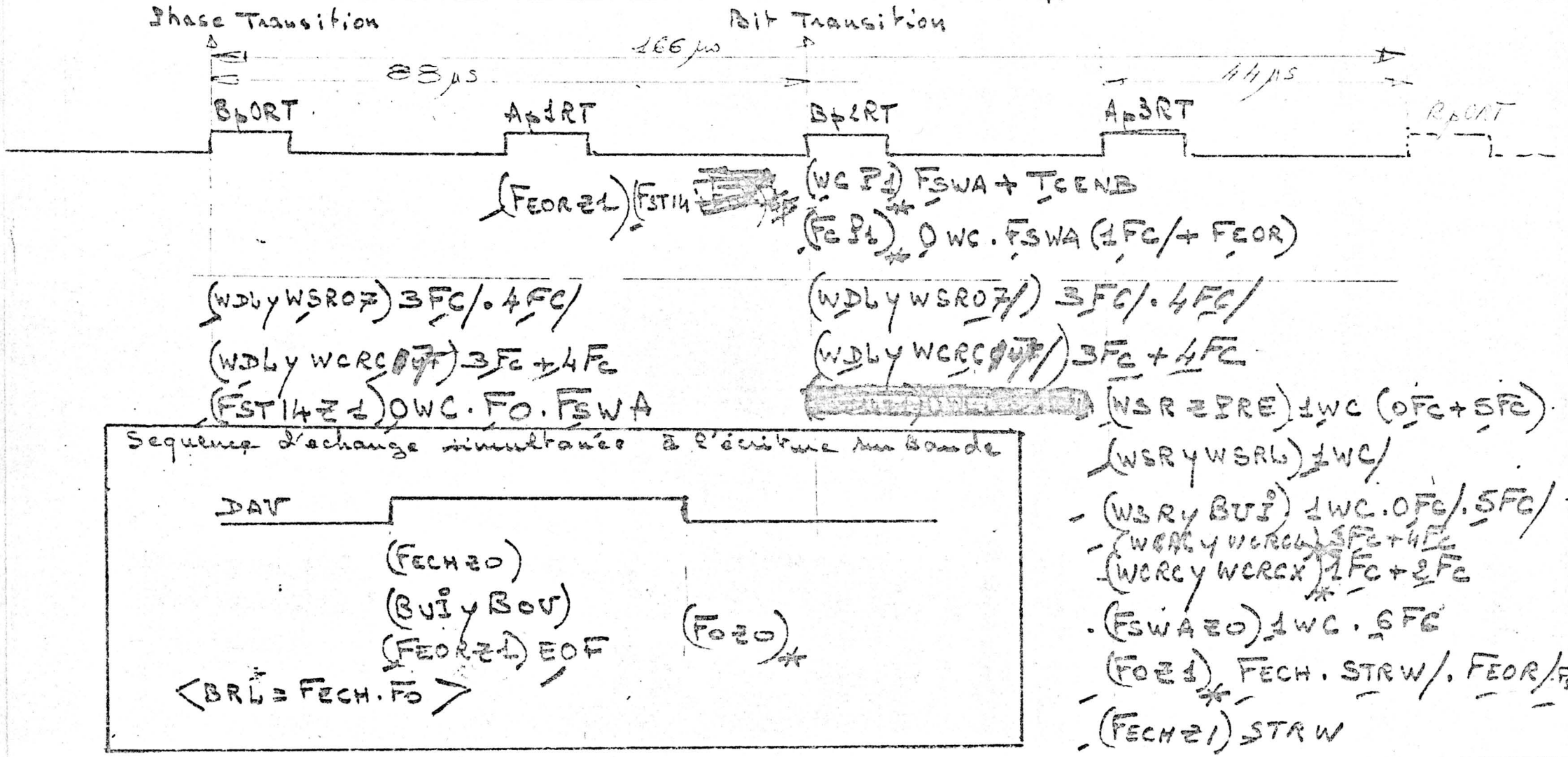
Table 3.6. Cable Connections CU And Device Nrs. 2 And 3.

Signal	Card KD Pin Nr.	Cable J2 Pin Nr.	Signal	Card KD Pin Nr.	Cable J2 Pin Nr.
WUN2*	5A06	1	FAST3*	5A15	14
WUN3*	5A05	2	LCK2*	5A21	15
BET2/*	5A09	3	LCK3*	5A22	16
BET3/*	5A10	4	CIP2/*	5A07	17
RCD2*	5A13	5	CIP3/*	5A08	34
RCD3*	5A14	6	RDY2/*	5A04	35
WCD2*	5A20	7	RDY3/*	5A03	36
WCD3*	5A23	8	A2/*	5A12	37
RDA2/*	5A24	9	A3/*	5A11	38
RDA3/*	5A25	10	REV2*	5A02	39
WDL2/*	5A19	11	REV3*	5A01	40
WDL3/*	5A18	12	FWD2*	5A17	41
FAST2*	5A16	13	FWD3*	5B01	42

equence WRITE SERIALISATION

Sequence de controle de la Sérialisation des données enregistrées

condition d'entrée : FSWA=1
condition initiale : WCRC = 0
WC = 1
demarage sur AB3RT

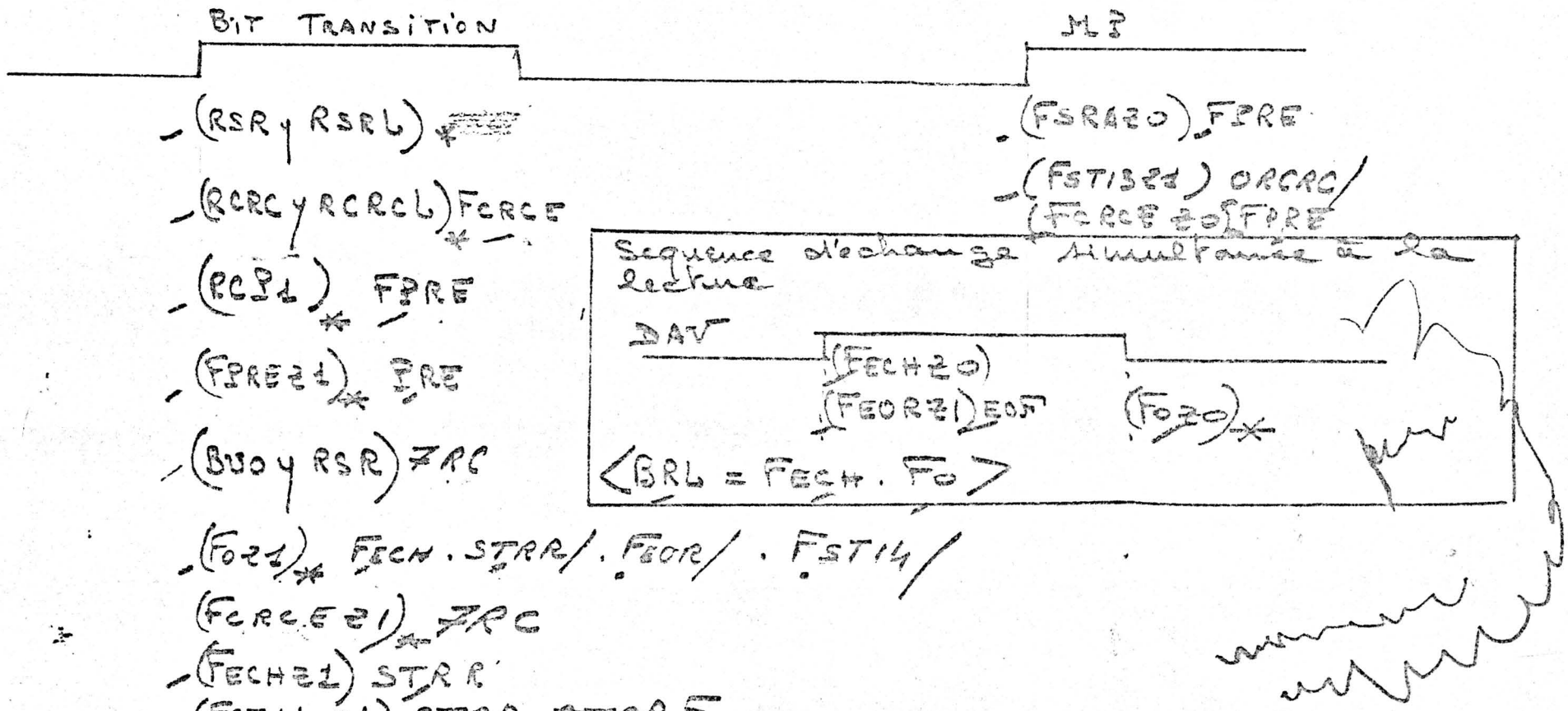


WSR = WSR00/---/WSR07 : writing shift register
FC = FC0/FC1/FC2 : Format counter - Modulo 6
3FC = 0/0/0 : ecriture preambule
4FC = 1/0/0 : ecriture data sauf dernier octet
5FC = 0/1/0 : ecriture dernier octet
6FC = 1/1/0 : ecriture CRC
WDL = WRITE Data
WCRCOUT = Write CRC F.F.
BUI = BUI00/----/BUI07 Buffer d'entrée
WCRC = WCRC01/----/WCRC16/WCRCOUT
PRE = 1/0/1/0/1/0/1/0 LSB PREAMBLE et POSTAMBLE
3FC = 1/0/1 Enregistrement écriture POSTAMBLE
4FC = 0/1/1 Fin seq. écriture
WDL = WRITE Data
WCRCOUT = Write CRC F.F.
BUI = BUI00/----/BUI07 Buffer d'entrée
WCRC = WCRC01/----/WCRC16/WCRCOUT
PRE = 1/0/1/0/1/0/1/0 LSB PREAMBLE et POSTAMBLE

Sequence READ SERIALIZATION

Sequence de contrôle de la sérialisation des données lues
Sequence fonctionnant simultanément avec l'écriture.

condition d'entrée : FSRA = 1
condition initiale :



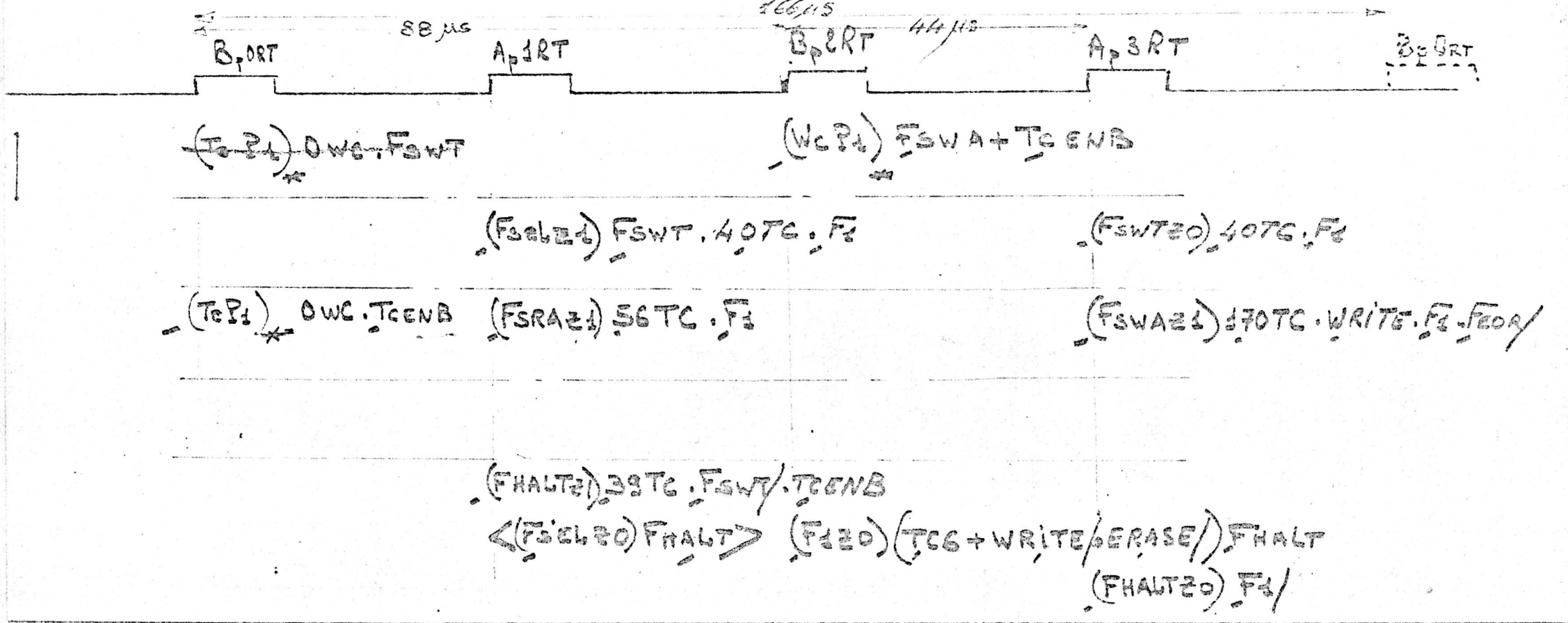
STRR = READ . FRC . RD/ . BT

Sequence EXECUTE | Sequence autonome

Controle des temps d'attente, de démarrage et d'arrêt tout au long de toutes les opérations

condition d'entrée : $F_1 = 1$ et FSWT = 1

condition initiale : TC = 0



TC = TC0/.../TCF Time counter

40TC = TC5

56TC = TC2 . TC5 . TC5

39TC = 1/1/1/1/1/0/0/0

170TC = TC7

WC = WC0/WC1/WC2 Write counter modulo 8

OWC = 0/0/0

FSWT = Start waiting time F.F.

FSWA = Start write time F.F.

TCENB = FSWT + Read . FSRA/ + WRITE . FSWA/ + ERASE + BCKSP . F

FSRA = Read ed F.F.

FHALT =

FSEL = AUTORISATION Demarrage cassette F.F

B

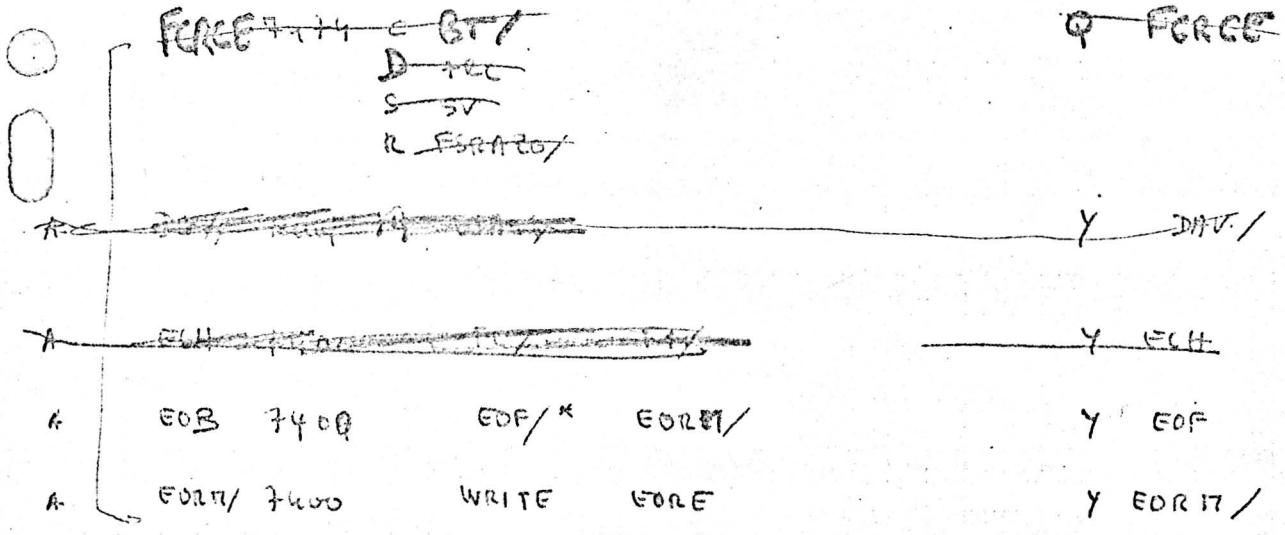
C	APBRT/	7400	AP	BRT	Y APBRT/
C	APBRT	7404	APBRT/		Y APBRT
A	BCKSP/	7402	SELECT/*	UNSEL/	Y BCKSP
A	BR/	7450	STROBE	WRITE READ	Y BR/
	B				
A	BRLW	7402	FO/	BRE	Y BRLW
A	BRL/	7404	BRLW		Y BRL/
	BTF/	7400	BT	FPRE	Y BTF/
	CLOCKBBL	7404	CLOCKFO/		Y CLOCKBBL
	CLOCKBBR	7404	CLOCKFO/		Y CLOCKBBR

BUI	7475	C	CLOCKBBL	Q1 BUI00
		D1	BOU00	Q2 BUI01
		D2	BOU01	
	7475	C	CLOCKBL	Q1 BUI02
		D1	BOU02	Q2 BUI03
		D2	BOU03	
	7475	C	CLOCKBL	Q1 BUI04
		D1	BOU04	Q2 BUI05
		D2	BOU05	
	7475	C	CLOCKBR	Q1 BUI06
		D1	BOU06	Q2 BUI07
		D2	BOU07	

BUO	7475	C	STRR	Q1 BUO00
		D1	RSR00	Q2 BUO01
		D2	RSR01	
	7475	C	STRR	Q1 BUO02
		D1	RSR02	Q2 BUO03
		D2	RSR03	
	7475	C	STRR	Q1 BUO04
		D1	RSR04	Q2 BUO05
		D2	RSR05	
	7475	C	STRR	Q1 BUO06
		D1	RSR06	Q2 BUO07
		D2	RSR07	

C CLOCK	7474	C	AP	Q ORT
		D	BRT	Q1 IRT
		S	5V	
		R	5V	
	7474	C	BP	Q IRT
		D	ORT	Q1 BRT
		S	5V	
		R	5V	

B card = Registers


FERCE 7474 C BT/
D FCC
S 5V
R FSRRTO/
Q FERCE
Y DRV/
Y ECH
A EOB 7408 EOF/* EORM/ Y EOF
A EORM/ 7400 WRITE EORE Y EORM/
A FEORE 7402 APERT/ FST14/ Y FEORE
Q FPRE 7474 C BT/ D PRE/ S F2 R 5V Q FPRE/ Q FPRE
FSTBZ1/ 7400 ORERC/ BCKSP/ Y FSTBZ1/
FSTBZ1/ 7474 C ηp D FSTBZ1/ S F1 R 5V Q FSTR/ Q FSTB
A FSTI4ZIA/ 7410 BPORT OWC FO FSWA Y FSTI4ZIA/
A FSTI4ZIB/ 7410 BT FO STRR Y FSTI4ZIB/
A FSTI4/ 7430 FSTI4 F1 Y FSTI4
A FSTI4 7410 FSTI4/ FSTI4ZIA/ FSTI4ZIB/ Y FSTI4
C PRE/ 7430 RSR00 RSR04 RSR01 RSR05 RSR02 RSR06 RSR03 RSR07 Y PRE/
RC 74193 COP BTF/ CDO 5V DA 5 DB 5 DC 5 DD 5 BO 5 LD 5 CL F1/ QA RC0 QB RC1 QC RC2
RCRC
E READ 7402 READ/ UNSEL/ Y READ

RCRC0102 7402 RCRC01 RCRC02 Y RCRC0102

RCRC0304 7402 RCRC03 RCRC04 Y RCRC0304

RCRC0506 7402

07 08	02
09 10	02
11 12	02
13 14	02
15 16	02

RDA/ 7404 RDA Y RDA/

RSR07/ 7404 RSR07 Y RSR07/

RSR 74164 C BT/
SA RDA
SA RDA
CL F1
QA RSR00
QB 01
QC 02
QD 03
QE 04
QF 05
QG 06
QH 07

1 STROBE 7404 STROBE/ Y STROBE

STRR/ 7410 BT FRC READ RDA/ Y STRR/

1 STRRW 7400 STRW/ STRR/ Y STRRW

A STR/ 7450 BRL READ Y STR/

STROBE WRITE

A STRW/ 7410 APBRT AWC FSWA Y STRW/

WLRC

WDL 7474 C BP
D WD
R FSWA
S 5V
Q WDL

WDX/ 7450 A WSR07 34FC/ Y WDX/
WGRC17 34FC

WDX 7404 A WDX/ Y WDX

WD 7450 ORT WDX/ Y WD

2RT WDX

R WRITE/ 7404 WRITE

A WRITE 7402 ~~WGATE/~~ EGR UNSEL/ Y WRITE

WSRD	9322	IOA	BUI00	ZA	WSRD00
	74157	I1A	5V	ZB	01
		IOB	BUI01	ZC	02
		I1B	0V	ZD	03
		IOC	BUI02		
		I1C	5V		
		IOD	BUI03		
		I1D	0V		
		S	05FC		
		E	0V		
	9322	IOA	BUI04	ZA	WSRD04
	74157	I1A	5V	ZB	05
		IOB	BUI05	ZC	06
		I1B	0V	ZD	07
		IOC	BUI06		
		I1C	5V		
		IOD	BUI07		
		I1D	0V		
		S	05FC		
		E	0V		

WSR07/	7404	WSR07		Y WSR07/
WSR	74166	CA	AP3RT/	QH WSR07
		CB	0V	
		SI	5V	
		PA	WSRD00	
		PB	WSRD01	
		PC	02	
		PD	03	
		PE	04	
		PF	05	
		PG	06	
		PH	07	
		SL	1WC/	
		CL	5V	

ORCRC/	7430	RCRC0102	RCRC0304	RCRC0506	RCRC0708	Y ORCRC/
		RCRC0910	RCRC1112	RCRC1314	RCRC1516	
12FC	7400	1FC/	2FC/			Y 12FC
34FC/	7404	34FC				
7RC/	7410	RC0	RC1	RC2		Y 7RC/
7RC	7404	7RC/				

RCRC	74175	C	BT/		QA	RCRC01
		DA	RFEED		QB	RCRC02
		DB	RCRC01		QB/	RCRC02/
		DC	RCRC16X		QC	RCRC16
		DD			QC/	RCRC16/
		R	FCRCF			
	74164	C	BT/		QA	RCRC03
		R	FCRCF		QB	RCRC04
		A	RCRC03X		QC	RCRC05
		B	RCRC03X		QD	RCRC06
					QE	RCRC07
					QF	RCRC08
					QG	RCRC09
					QH	RCRC10
	74164	C	BT/		QA	RCRC11
		R	FCRCF		QB	RCRC12
		A	RCRC[illegible]		QC	RCRC13
		B	RCRC[illegible]		QD	RCRC14
					QE	RCRC15
RFEED/	7404	A	RFEED		Y	RFEED/
RFEED	7450	A	RCRC16	RSR07	Y	RFEED
		A	RCRC16/	RSR07/		
RCRC03X	7450	A	RCRC02	RFEED	Y	RCRC03X
		A	RCRC02/	RFEED/		
RCRC16X	7450	A	RCRC15	RFEED	Y	RCRC16X
		A	RCRC15/	REED/		

WCRC	74175	C	AP3RT/		QA	WCRC01
		DA	WFEED		QB	WCRC02
		DB	WCRC01		QB/	WCRC02/
		DC	WCRC16X		QC	WCRC16
		DD	WCRC16		QC/	WCRC16/
		R	FSWA		QD	WCRC17
					QD/	WCRC17/
	74164	C	AP3RT/		QA	WCRC03
		R	FSWA		QB	WCRC04
		A	WCRC03X		QC	WCRC05
		B	WCRC03X		QD	WCRC06
					QE	WCRC07
					QF	WCRC08
					QG	WCRC09
					QH	WCRC10
	74164	C	AP3RT/		QA	WCRC11
		R	FSWA		QB	WCRC12
		A	WCRC10		QC	WCRC13
		B	WCRC10		QD	WCRC14
					QE	WCRC15
WFEED/	7400	A	WFEEDX	12FC	Y	WFEED/
WFEED	7404	A	WFEED		Y	WFEED
WFEEDX	7450	A	WCRC16	WSR07	Y	WFEEDX
		A	WCRC16/	WSR07/		
WCRC03X	7450	A	WCRC02	WFEED	Y	WCRC03X
		B	WCRC02/	WFEED/		
WCRC16X	7450	A	WCRC15	WFEED	Y	WCRC16X
		A	WCRC15/	WFEED/		

LISTE LOGIQUE CARTE A.

C APREADY	7408	A	AP	RDY			Y	APREADY
BRL/	7404	A	BRL#				Y	BRL/
BRL	7402	E	FO/	BRE/			Y	BRL
BR/	7450	E	BRL	FWRITE			Y	BR/
		A	STROBE	FREAD				
BRE/	7400	A	FECH	FEOR/			Y	BRE/
BRE	7404	A	BRE/				Y	BRE
CFC/	7420	A	BP	2RT	OWC	FCE	Y	CFC/
CLOCKFO/	7404	A	CLOCKFO				Y	CLOCKFO/
C CLOCKFO	7402	E	DAV/	UNSEL/			Y	CLOCKFO
CWCW/	7400	A	BP2RT	TCE			Y	CWCW/
DEBW	7402	E	FWRITE/	TC7/			Y	DEBW
EOB	7400	A	EOF/	EORT/			Y	EOB
EORE	7404	A	EORE/				Y	EORE
EORT/	7400	A	FWRITE	EORE			Y	EORT/
CFERASE/	7474	D	FERASE/ SV				Φ	FERASE / Φ/ FERASE/
CERASE	7408	C	EFF/ ERASE/	UNSEL/			Y	ERASE
CERW.	7402	C	FERASE/	WUN			Y	ERW

FCE	7402	C	FSWA/	1FCEOR/			Y	FCE
FC	74193	CUP	CFC/				QA	FC0
		CDO	5V				QB	FC1
		DA	5V				QC	FC2
		DB	5V					
		DC	5V					
		DD	5V					
		LD	5V					
		BO	5V					
		CL	F1/					
FECH/	7410	A	FECH	CLEAR/	CLOCKFO/		Y	FECH/
FECH	7400	A	FECH/	STRRW/			Y	FECH
FEORE	7402	C	APIRT/	FSTI4/			Y	FEORE
FEOR21/	7450	A	F1	EOB			Y	FEOR21/
		A	F1	FEORE				
FEOR/	7400	A	FEOR	F1			Y	FEOR/
FEOR	7400	A	FEOR/	FEOR21/			Y	FEOR
FHALT20/	7400	A	AP	F1/			Y	FHALT20/
FHALT21/	7420	A	AP	FSWT/	39TC	TCE	Y	FHALT21/
FHALT/	7400	A	FHALT	FHALT20/			Y	FHALT/
FHALT	7400	A	FHALT/	FHALT21/			Y	FHALT

```
FSRAZ0/   7400  A  NP    FPRE                      Y FSRAZ0/
FSRAZ1/   7410  A  AP    RTC     F1                Y FSRAZ1/
FSRA/     7410  A  FSRA  CLEAR/  FSRAZ0/           Y FSRA/
FSRA      7400  A  FSRA/ FSRAZ1/                   Y FSRA
FST14Z1A/ 7420  A  BPORT OWC     F0      FSWA      Y FST14Z1A/
FST14Z1B/ 7410  A  BT    F0      STRR              Y FST14Z1B/
FST14/    7400  A  FST14 F1                        Y FST14
FST14     7410  A  FST14/ FST14Z1A/ FST14Z1B/      Y FST14
FSWAZ0/   7410  A  APBRT IWC     6FC               Y FSWAZ0/
FSWAZ1/   7420  A  APBRT DEBW    F1      FE0R/     Y FSWAZ1/
FSWA/     7410  A  FSWA  CLEAR/  FSWAZ0/           Y FSWA/
FSWA      7400  A  FSWA/ FSWAZ1/                   Y FSWA
FSWTZ0/   7410  A  APBRT TC5     F1                Y FSWTZ0/
FSWT/     7400  A  FSWT  FSWTZ0/                   Y FSWT/
FSWT      7400  A  FSWT/ F1                        Y FSWT
```

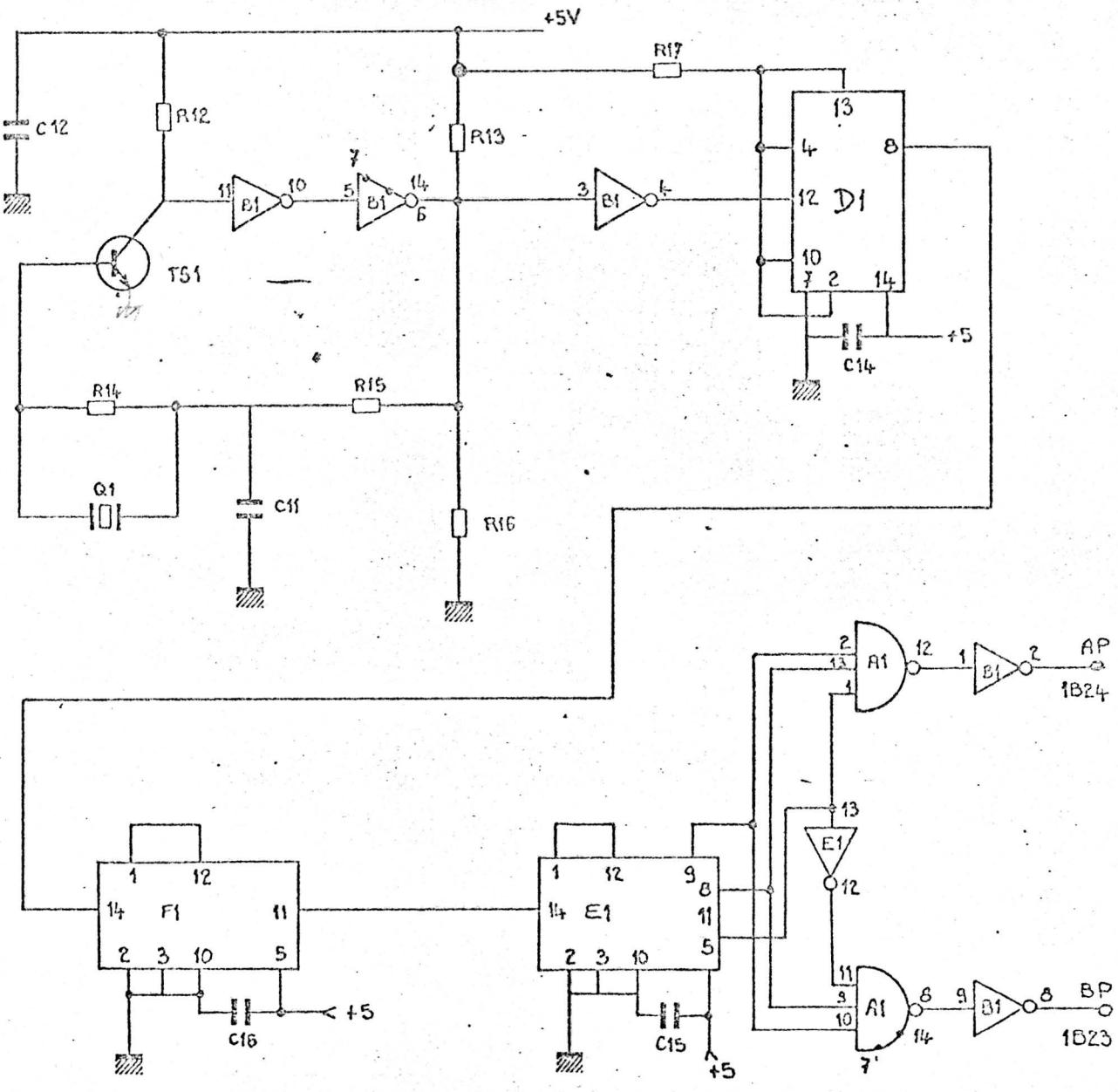
F0	7476	C	CLOCKF0				Q	F0
		J	0V				Q/	F0/
		K	5V					
		S	GOTOECH/					
		R	RESETF1/					
F1Z1/	7453	A	APREADY	BCKSP			Y	F1Z1/
		A	APREADY	ERW				
		A	APREADY	WRW				
		A	APREADY	REM				
F1	7476	C	5V				Q	F1
		J	5V				Q/	F1/
		K	5V					
		S	F1Z1/					
		R	RESETF1/					
GOTOECH/	7420	A	BRF	STRRW/	FST14/	CLOCKF0/	Y	GOTOECH/
GOTOINCT/	7420	A	BP	FHALT	TCG	CLOCKF0/	Y	GOTOINCT/
RESETF1/	7404	A	RESETF1				Y	RESETF1/
RESETF1	7400	A	GOTOINCT/	CLEAR/			Y	RESETF1
REM/	7400	A	READ	EMPTYAB			Y	REM/
REM	7404	A	REM/				Y	REM
RTC/	7410	A	TC5	TC3	TC2		Y	RTC/
RTC	7404	A	RTC/				Y	RTC

STROBE	7404	A	STROBE/			Y	STROBE
STRRW	7400	A	STRR/	STRW/		Y	STRRW
~~STRR/~~	~~7410~~	~~A~~	~~BT~~	~~IRC~~	~~READ~~	~~Y~~	~~STRR/~~
STRW/	7410	A	APSRT	IWC	FSWA	Y	STRW/
STR/	7450	A	BRL	READ		Y	STR/
		A	STROBE	WRITE			
TCC/	7410	A	BPORT	OWC	TCE	Y	TCC/
TCENB/	7453	A	READ	FSRA/		Y	TCENB/
		A	BCRSP	FSRA/			
		A	WCD	WCD			
		A	FSWT	FSWT			
TCE	7404	A	TCENB/			Y	TCE
TCRR	7400	A	F1	BT/		Y	TCRR
TC5/	7404	A	TC5			Y	TC5/
~~TC6END~~	~~7400~~	~~A~~	~~TC6/~~	~~WCD~~		~~Y~~	~~TC6END~~
TC6/	7404	A	TC6			Y	TC6/
TC7/	7404	A	TC7			Y	TC7/

TC	74193	CUP	TCC/		QA	TC0
		CD0	5V		QB	TC1
		DA	5V		QC	TC2
		DB	5V		QD	TC3
		DC	5V		CA	TCOVF
		DD	5V			
		LD	5V			
		BO	5V			
		CL	TCTR			
	74193	CUP	TCC/		QA	TC4
		CD0	5V		QB	TC5
		DA	5V		QC	TC6
		DB	5V		QD	TC7
		DC	5V			
		DD	5V			
		LD	5V			
		BO	TCOVF			
		CL	TCTR			
C WLD	7400	A	ERASE/	FWRITE/	Y	WLD
FWRITE/	7404	A	FWRITE		Y	WRITE/
C WRITE	7402	C	~~WRITE~~ ECR/	UNSEL/	Y	WRITE
WC	74193	CUP	CWCW/		QA	WC0
		CD0	5V		QB	WC1
		DA	5V		QC	WC2
		DB	5V		QD	
		DC	5V			
		DD	5V			
		LD	5V			
		BO	5V			
		CL	5V			

WRW/	7410	A	WRITE	WUN/	FOLAB		Y	WRW/	
# WRW	7404	A	WRW/				Y	WRW	
C WUN	7404	A	WUN/				Y	WUN	
OWC	7404	A	OWC/				Y	OWC/	
01WC	7442	A0	WC0				0/	0WC/	
		A1	WC1				1/	1WC/	
		A2	WC2						
		A3	OV						
01234567FC	7442	A0	FC0				0/	0FC/	
		A1	FC1				1/	1FC/	
		A2	FC2				2/	2FC/	
		A3	OV				3/	3FC/	
							4/	4FC/	
							5/	5FC/	
							6/	6FC/	
05FC	7400	A	0FC/	5FC/			Y	05FC	
1WC	7404	A	1WC/				Y	1WC/	
1FCEOR/	7402	C	1FC/	FEOR			Y	1FCEOR/	
12FC	7400	A	1FC/	2FC/			Y	12FC	
34FC	7400	A	3FC/	4FC/			Y	34FC	
39TC/	7430	A	TC7/	TC6/	TC5/	TC4	Y	39TC	
		A	TC3	TC2	TC1	TC0			
39TC	7404	A	39TC/				Y	39TC	

Write Circuit



5 MARS 1973

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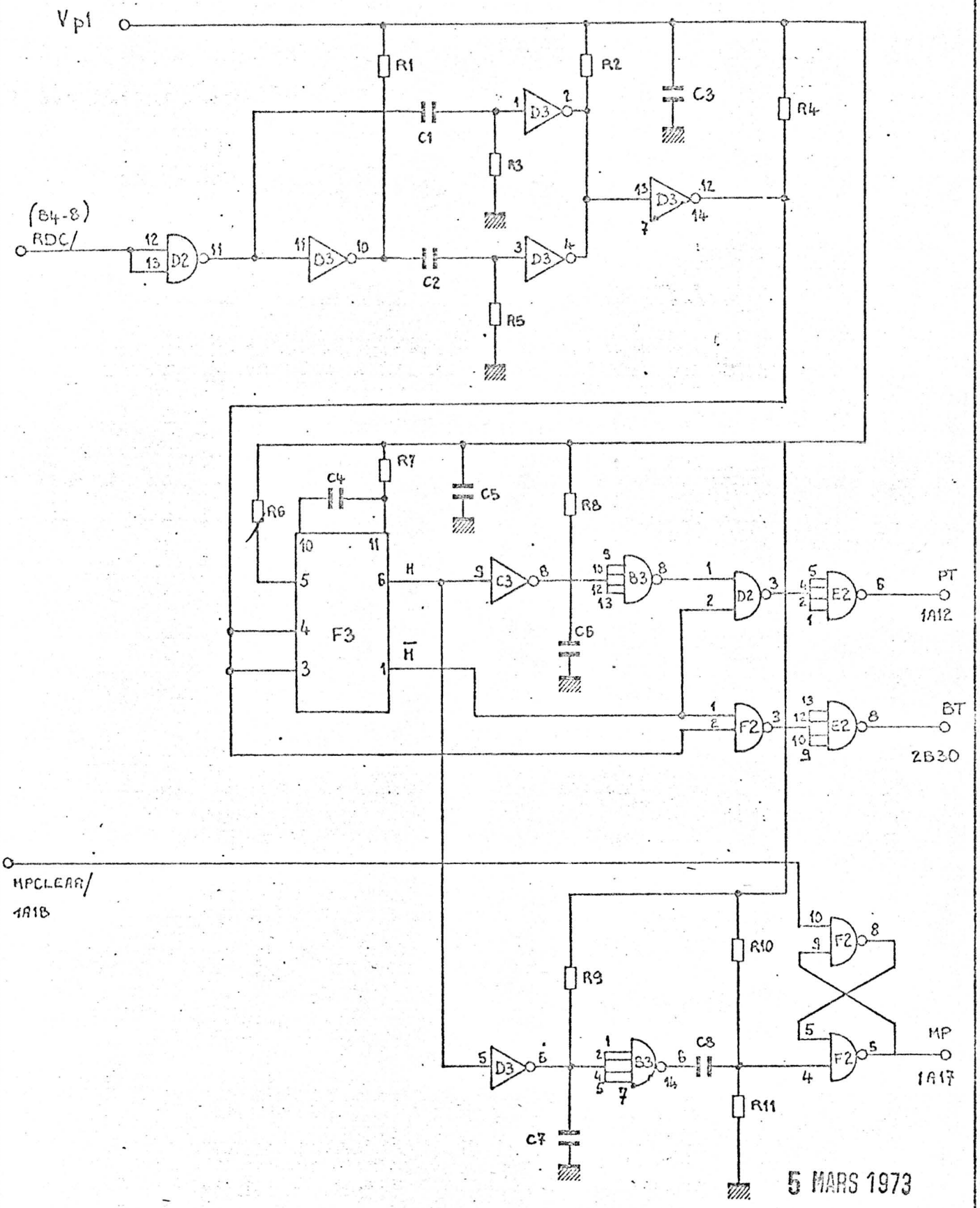
état 2	date	CARTE KD	5111 199 83900		7212.08	
état 1	date		Type de page : 130 page 9/6			

NAME NOM	BLANDIN	Philips Data Systems	Form A 4
CHECK CONTR		IGSC - Centre Technique et Industriel - Fontenay-aux-Roses - France	

Read Circuit



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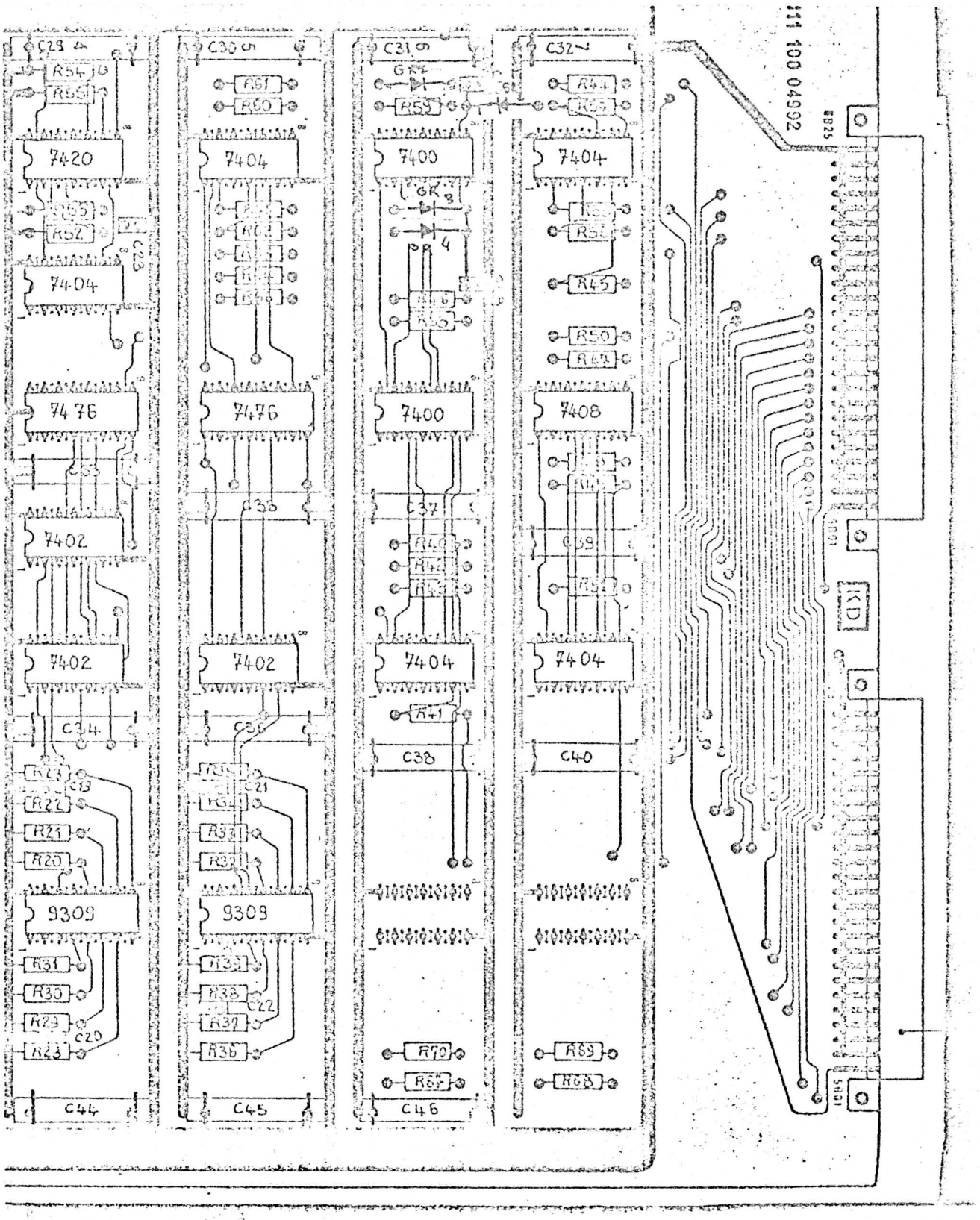
état 1	date		Type de page : 130 page 1/6			

NAME NOM BLANDIN	Philips Data Systems	Form A 4
CHECK CONTR	IGSC - Centre Technique et Industriel - Fontenay-aux-Roses - France	

PROJET SAG
COMPLEMENT DE LA PAGE 111
ELEMENT Contre Unit KF ELA X1710
N° CODE 5 111 13983 90.2

INDICE A
MODIF N° 1813
CARTE : KD

: les diodes GR1,2,3,4 remplacent les résistances R 82, 83, 84, 85



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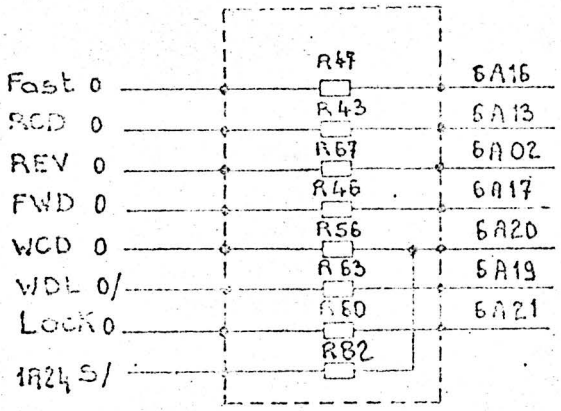

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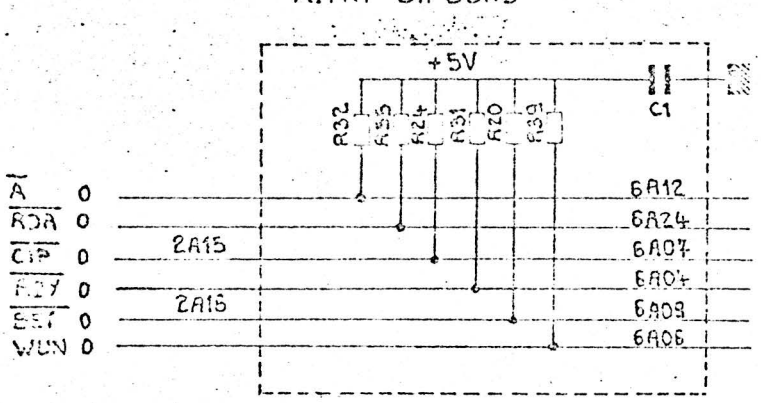

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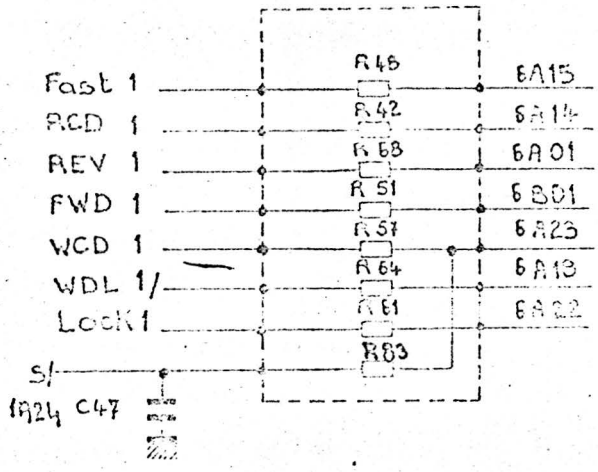
Start date 1		Type de page 130 6/6.		730328	1??
Author BLANDIN	Philips Data Systems				Form A 4
Check	IGSC - Centre Technique et Industriel - Fontenay-aux-Roses - France				

5111 091 00251

18 AVRIL 1973

A0KP Circuits



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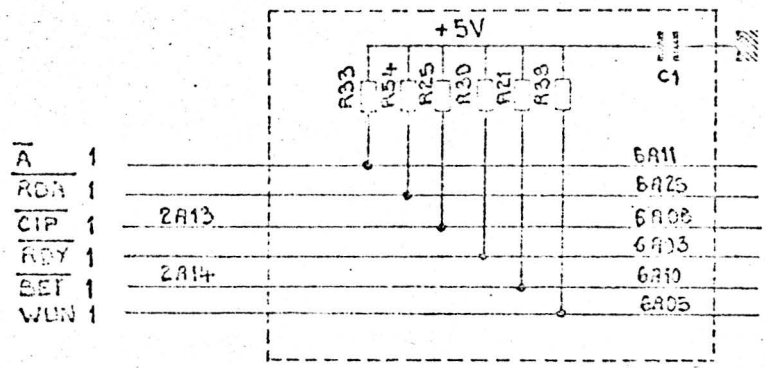

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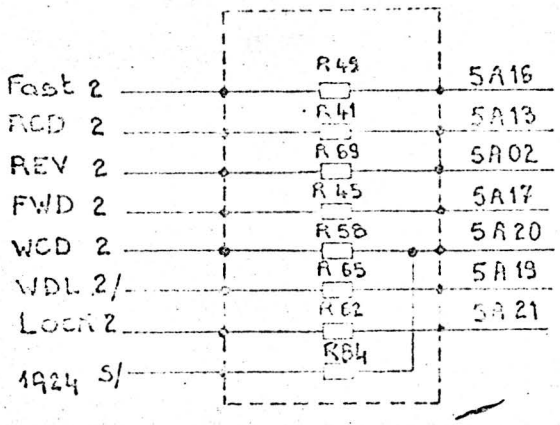
Stat 1		Type de page 130 Feuille 3/6		730328	1789
Visa BLANGIN	Philips Data Systems				Form A 4
Date	I.C.I.C - Centre Technique et Industriel - Fontenay-aux-Roses - France				

18 AVRIL 1973

A0KP Circuits



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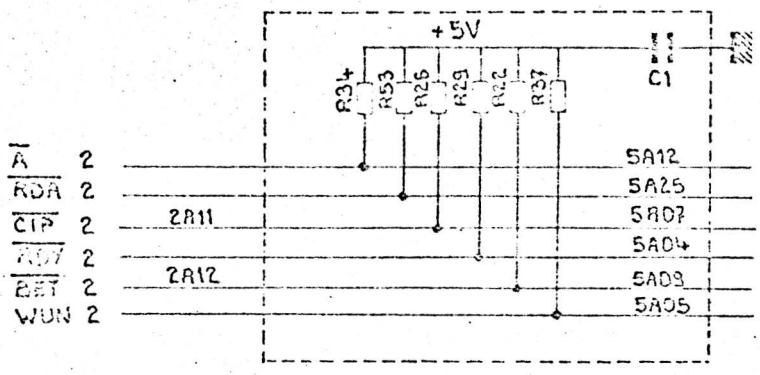
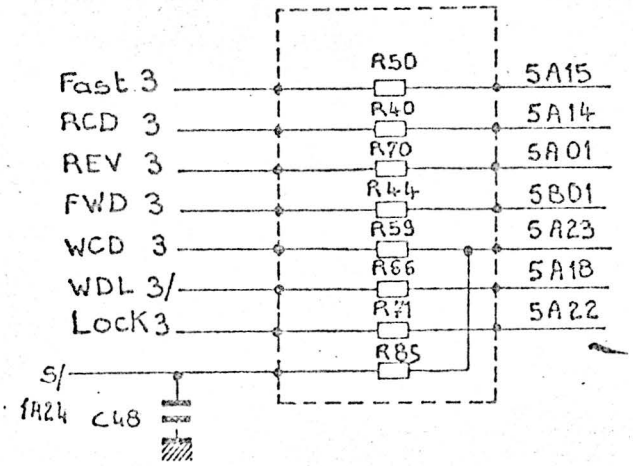


MATERIEL MATERIEL	TRAITEMENT TRAITEMENT			TOLERANCES	SCALE ECHELLE
Sht/Feuille 3	Description SAG	Code 12 NC	Nbre	Date	Check
Start/Début 2	CARTE KD	5111 199 83900		721208	
Start/Début 1		Type de page 130 Page 4/6		730328	1737
DES BLANDIN	Philips Data Systems				Form A 4
Check/Contrôle	IRIC - Centre Technique et Industriel - Fontenay-aux-Roses - France				

5111 991 00201

A0KP Circuits



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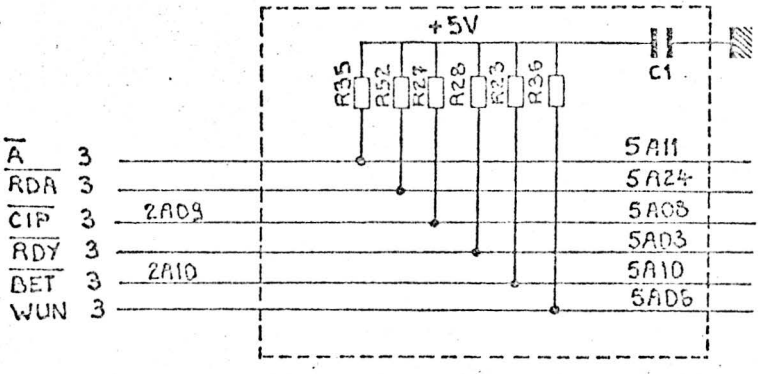

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état 1 / date		Type de page : 130 page 5/6		730328	1789
NOM CLANDIN / CHECK CONTR	Philips Data Systems IGSC - Centre Technique et Industriel - Fontenay-aux-Roses - France			Form A 4	

5111 991 00051

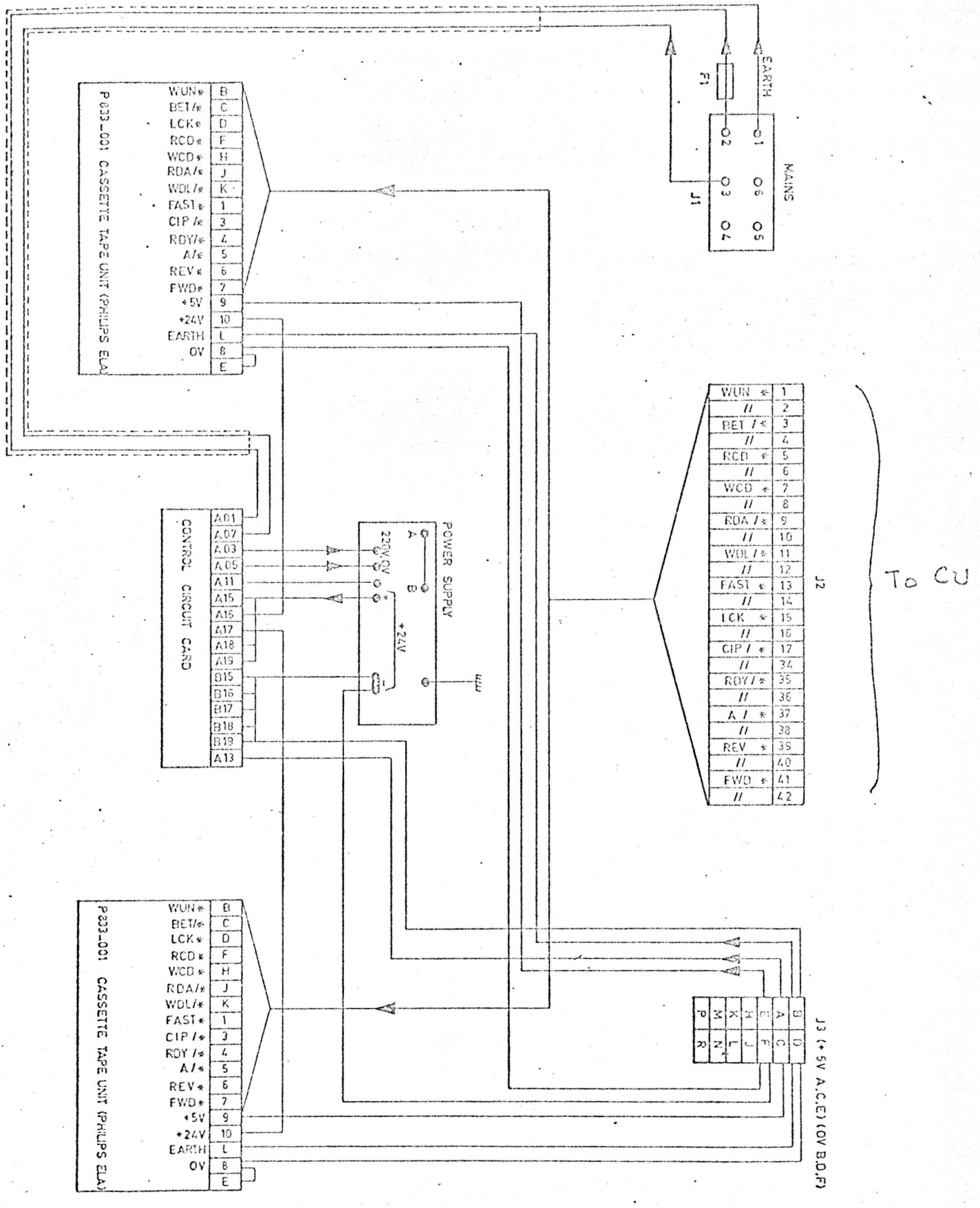


Figure 3.15 Cabling Between CU and Devices.

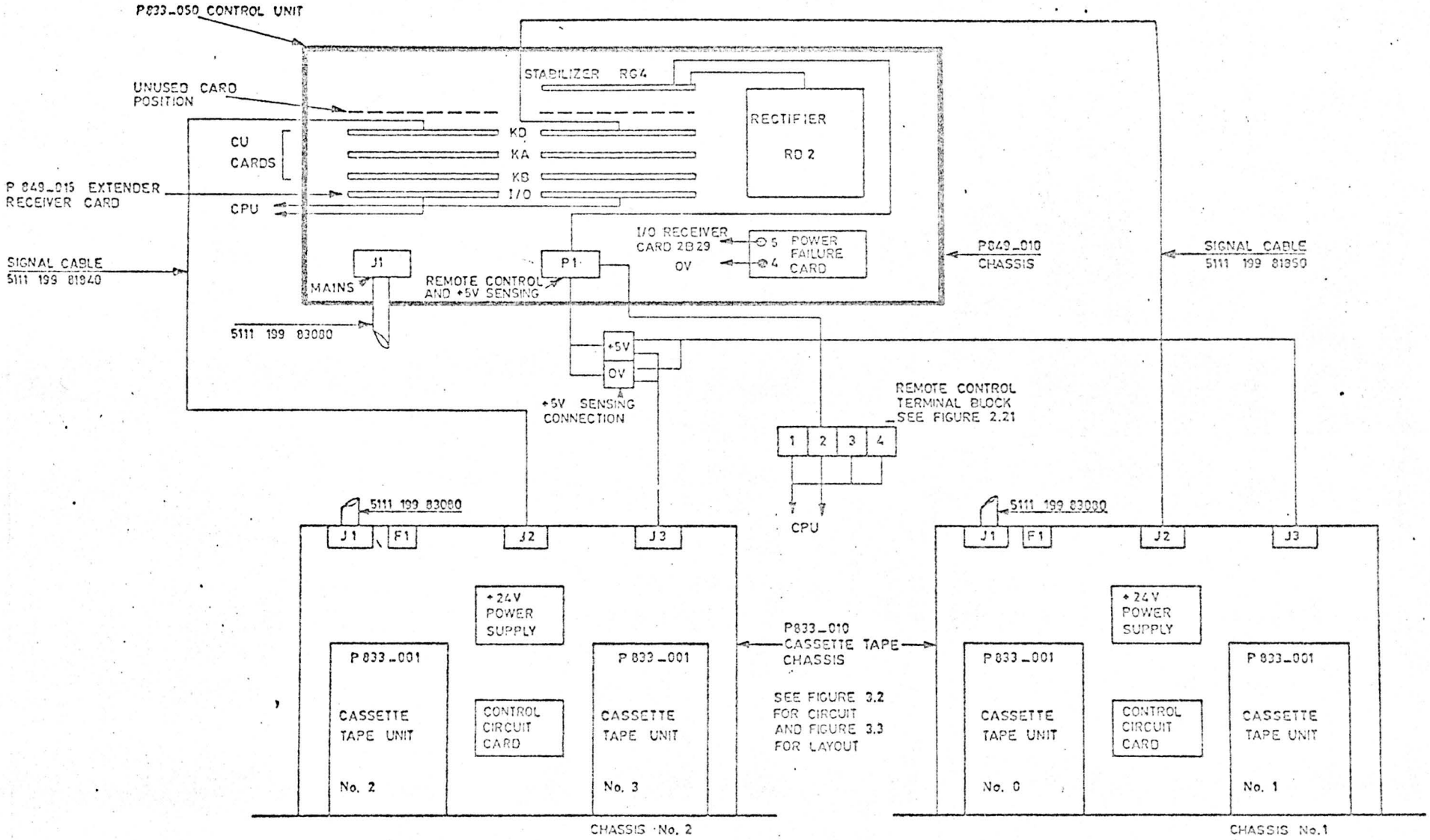


Figure 3.14 Cassette system layout and Cabling.

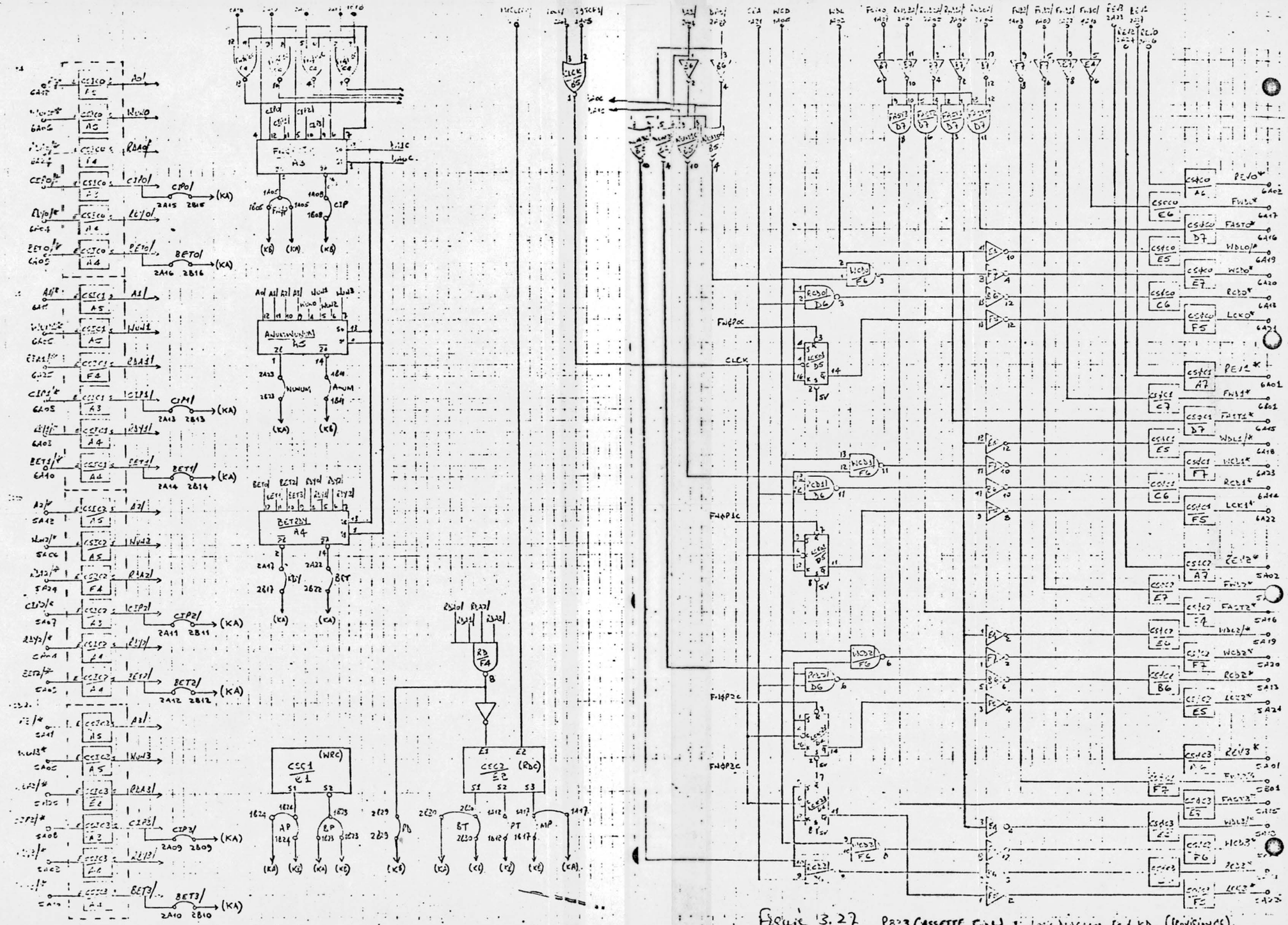


Figure 3.27 P823 CASSETTE C.P.U. : Logic Diagram (Provisional).

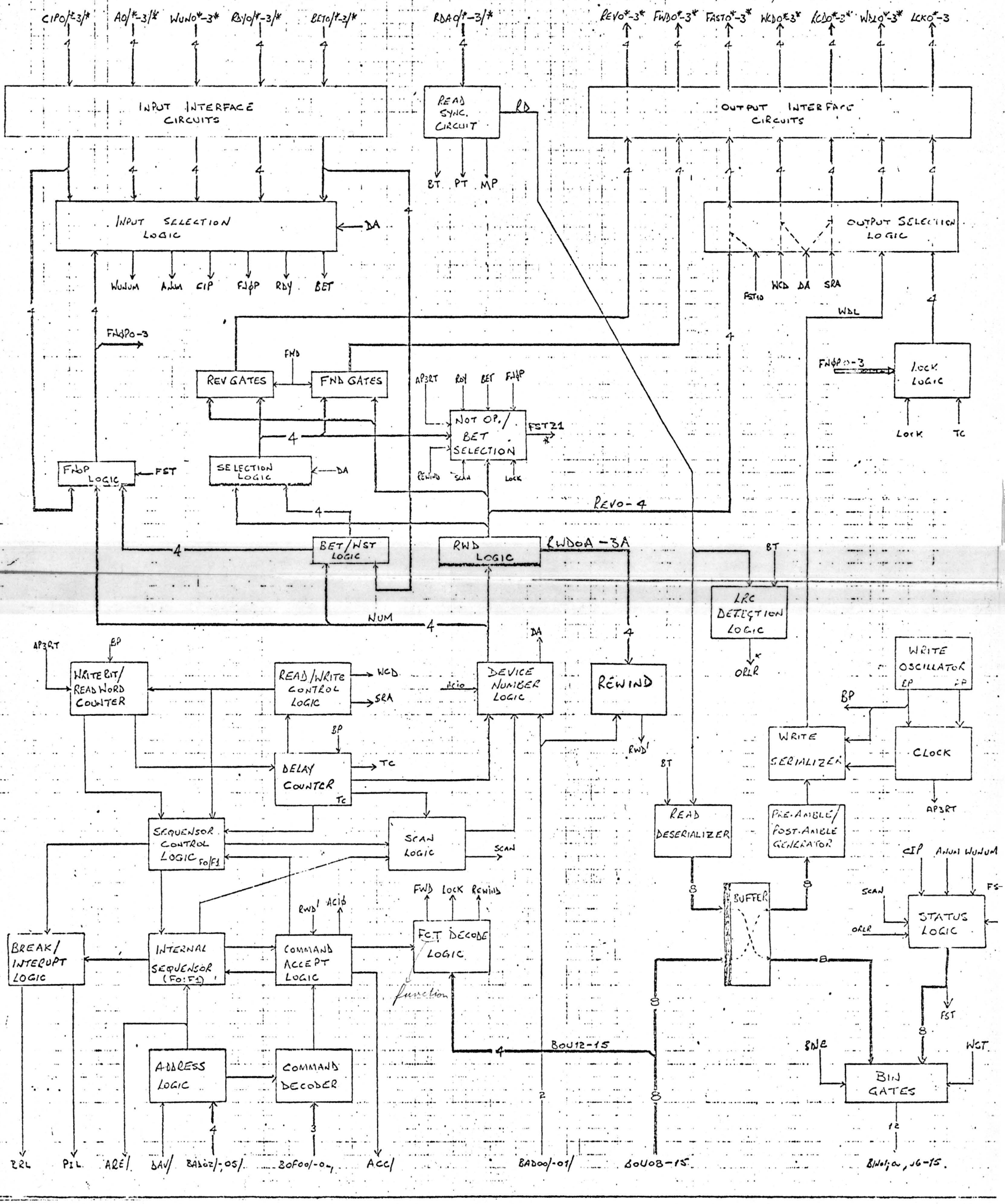


Figure 3.13 Page SCU Block Diagram

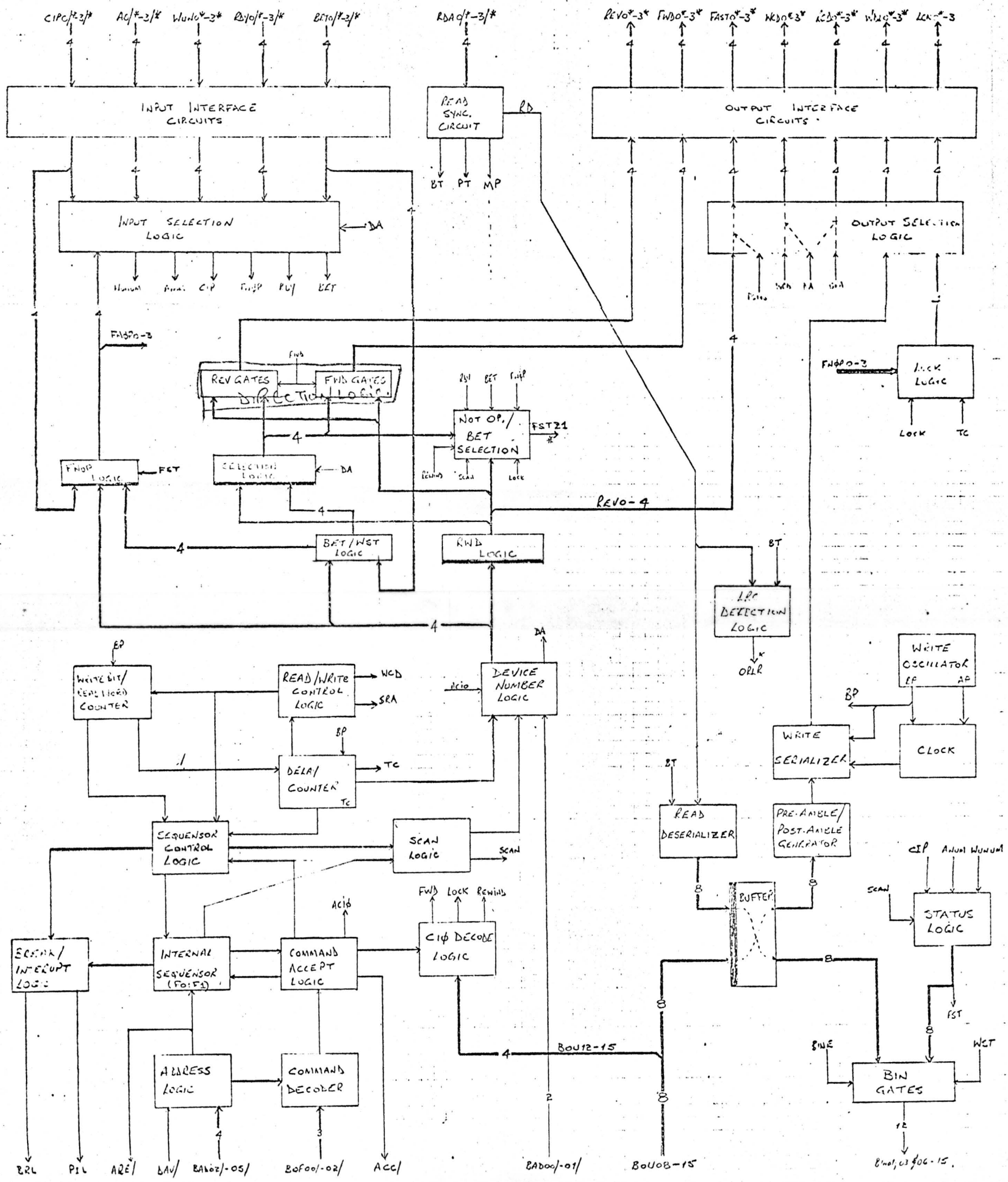


Figure 3.13. Block Diagram

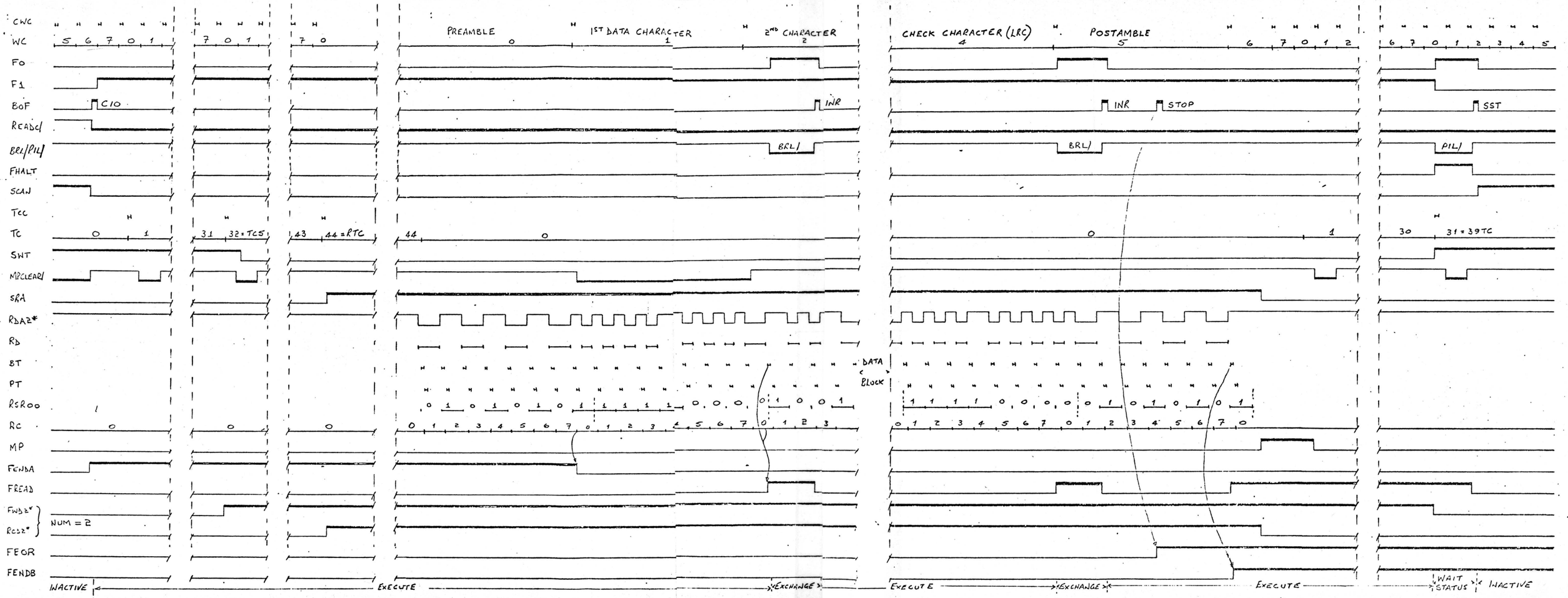
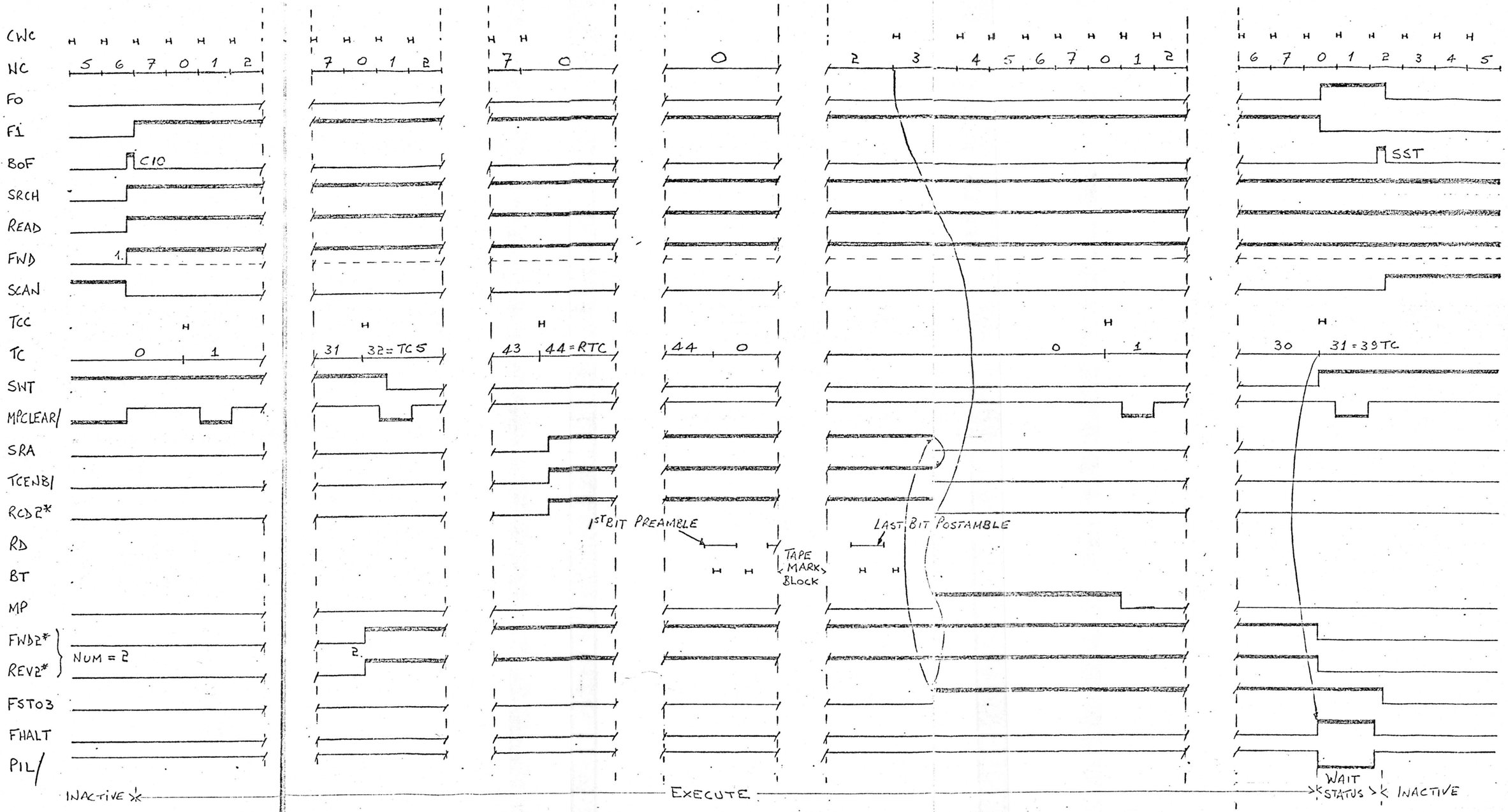
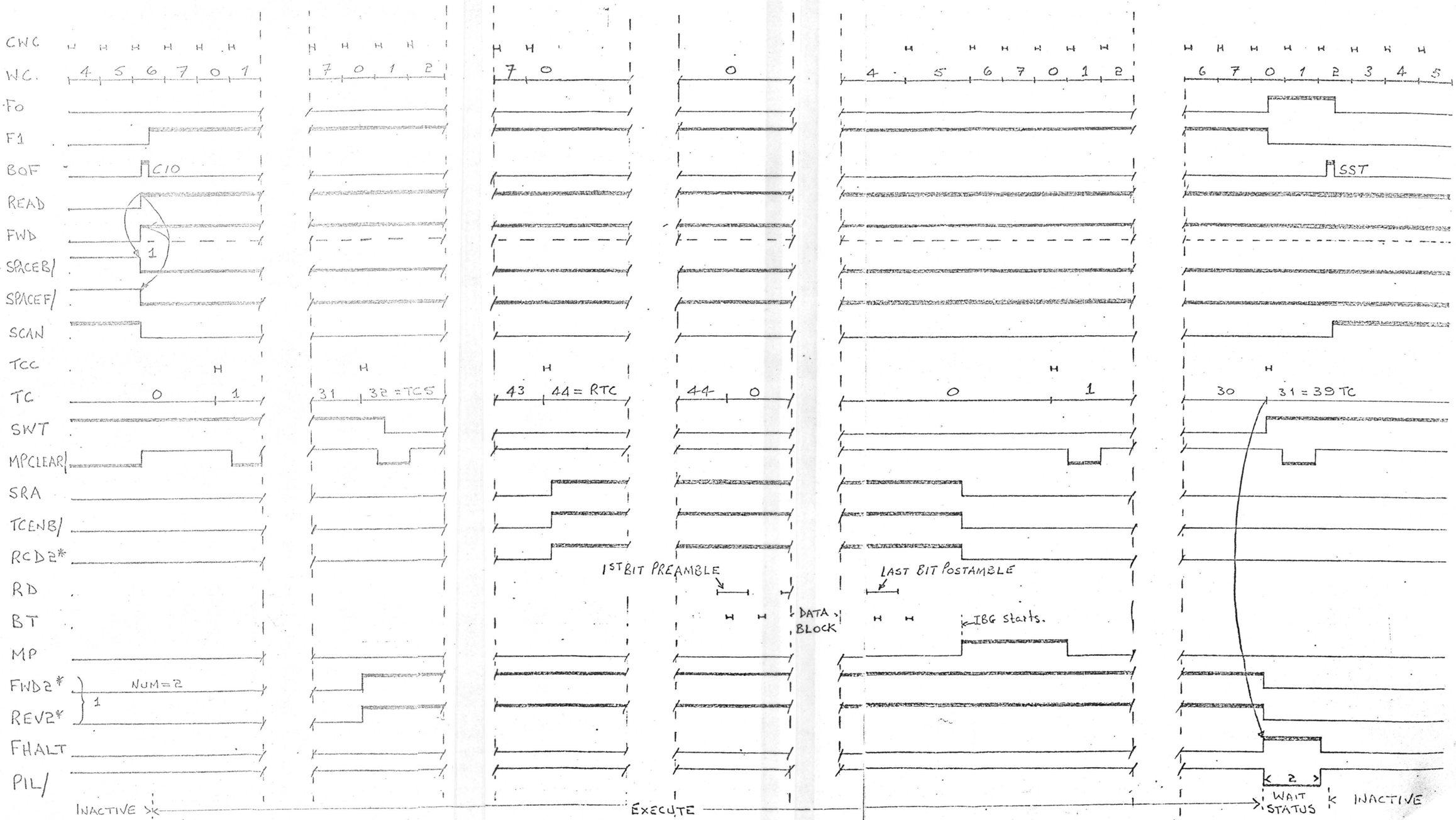


Figure 3.12. READ ONE BLOCK TIMING



NOTES: 1. Dependent on tape direction.
2. Select addressed cassette unit (Nr. 2).
3. Time dependent on central processor.

Figure 3.10. SEARCH TAPE MARK (FORWARD/BACKWARD).



NOTES: 1. The Space signal set is dependent on tape direction.
2. Time dependent on central processor.

Figure. 3.9. SPACE ONE BLOCK (FORWARD/BACKWARD).

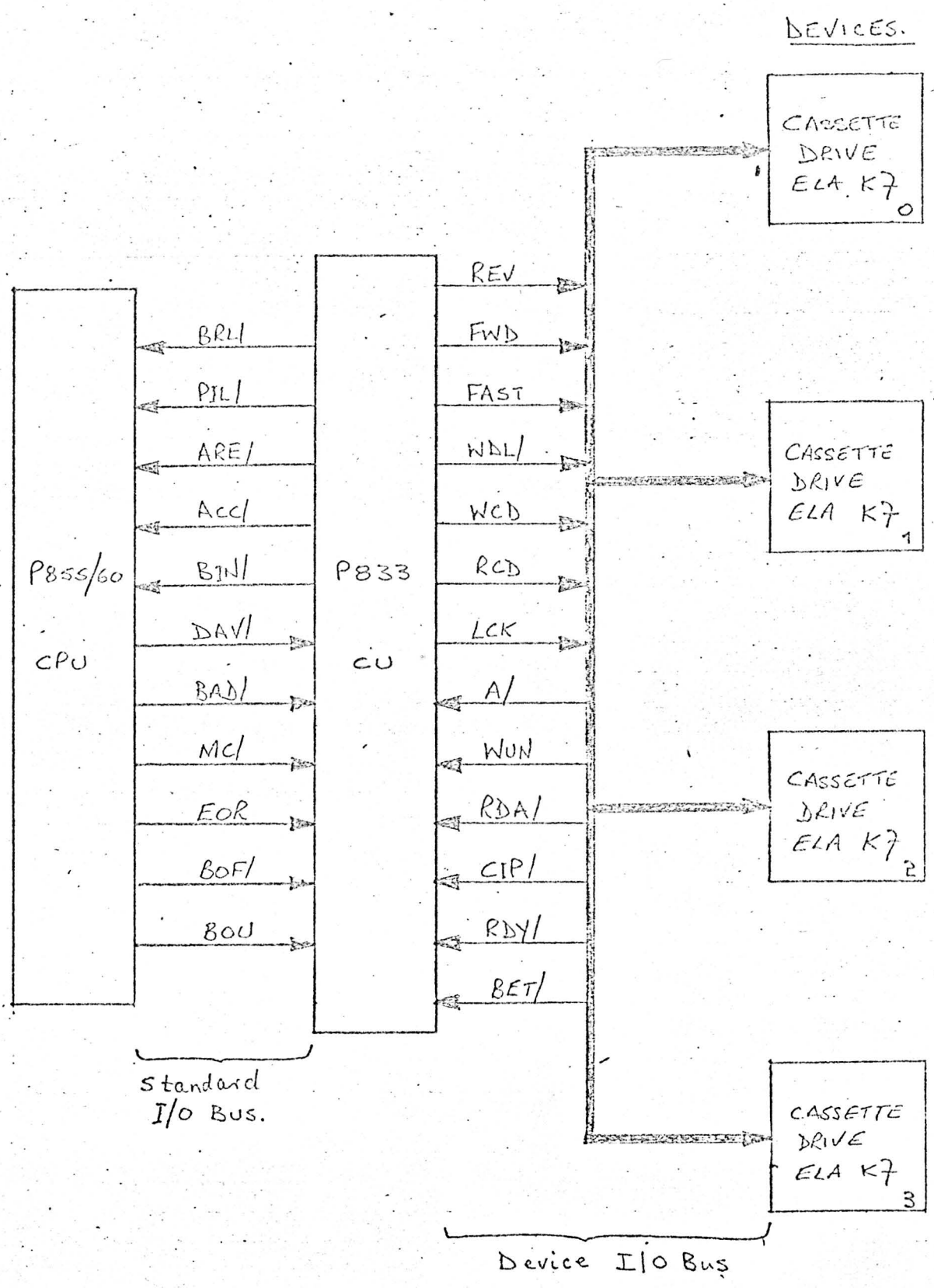
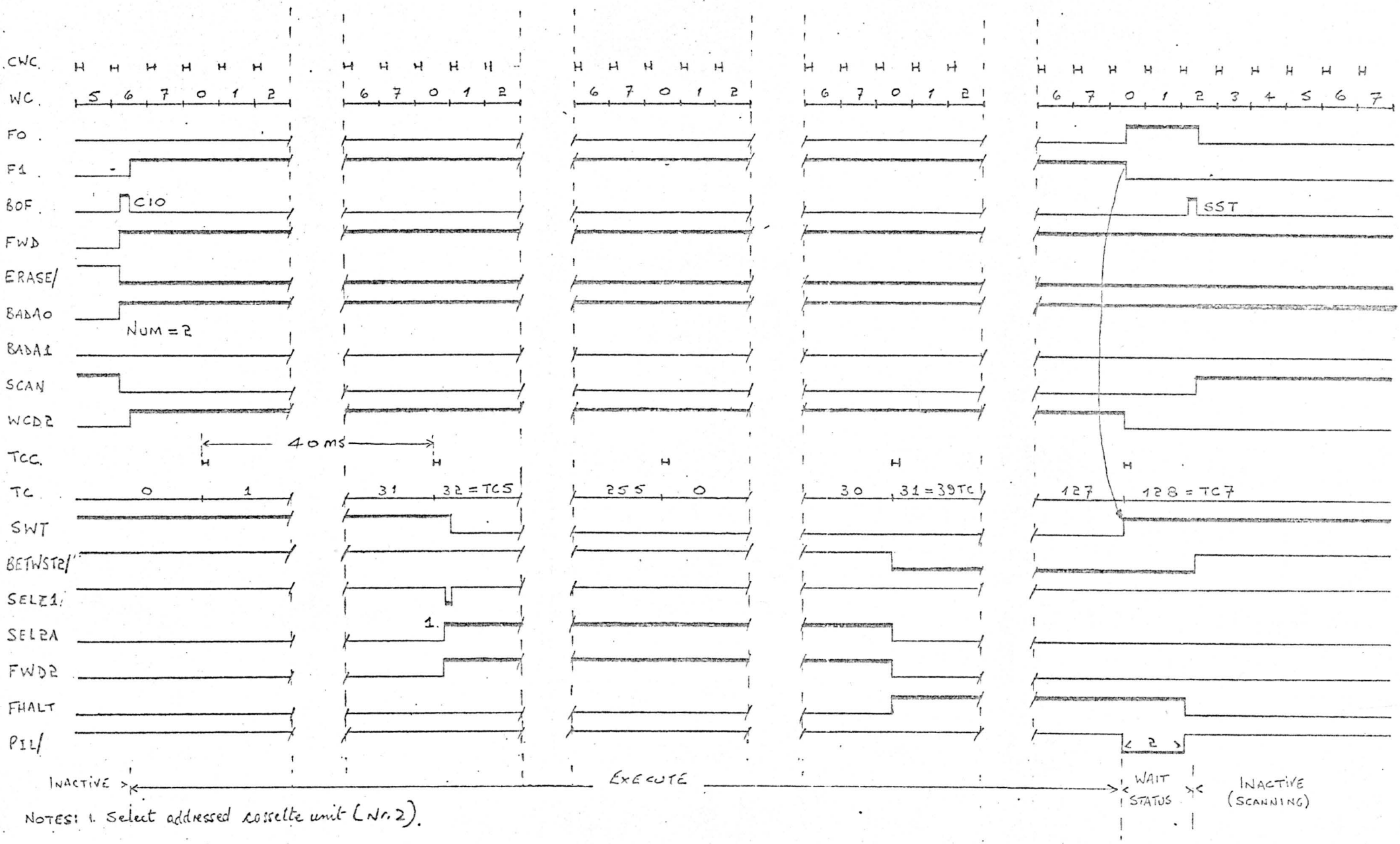


Figure 3.1. P855/60 Cassette Tape Subsystem Block Diagram.



NOTES: 1. Select addressed cassette unit (Nr. 2).

2 Time dependent on central processor.

Figure 3.8. ERASE TIMING.

Mnemonic	Description
LCK0 - LCK3	Lock flip-flops. Set or reset during a CIO LDCK command to lock or unlock the corresponding device depending on previous condition.
READ	Function flip-flop; set by BOU14 and indicates read or write operation.
RWD0A - RWD3A	Rewind flip-flops; indicate rewind condition on corresponding device.
SEL0A - SEL3A	Select flip-flops; memorize device selected.
SRA	Read flip-flop. Set at the start read time (RTC) and reset by MP when missing data condition is detected.
SRCH	Function flip-flop; set by BOU12 and indicates a search operation.
SWA	Write flip-flop. Set at start of Preamble serialization and removes inhibit from WDL; reset at end of Postamble serialization by ENDW.
SWT	Start delay flip-flop. Set by F1 when the CU goes to Wait Status or Inactive state; Reset approx. 40 msec (start delay) after an operation begins. The delay ensures that sufficient times elapses ~~between~~ after CIO commands to allow ~~status information to be sent to the CPU~~ direction change of motor tape and before reuse, tape stop after read operation; FAST
TRANS	Function flip-flop; set by BOU13 and indicates a data transfer operation.
WDL	Write data flip-flop. Driven by Write Serializer and is serial data on the Write Data line of the addressed device.